3D-Stacking of Ultra-Thin Chips and Chip Packages

3D-stapelen van ultradunne chips en chipverpakkingen

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Swarnakamal Priyabadini
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List of Acronyms

0-9

2D	Two dimensional
3D	Three dimensional

A

ACB	Advanced Circuit Boards
ASTRI	Applied Science and Technology Research Institute
ASIC	Application-specific integrated circuit

B

BGA	Ball Grid Array
BCB	Benzocyclobutene

C

CMST	Centre for Microsystems Technology
CIP	Chip in Polymer
CTE	Coefficient of Thermal Expansion

D

DI	Deionized
DFR	Dry Film Resist
DAF	Die Attach Film

E

EU FP7	European Union Frame-Work 7
EEPROM	Electrically Erasable Programmable Read-Only Memory
EDX	Energy-dispersive X-ray spectroscopy
ESD	Electrostatic Discharge

F

FBGA	Fine-pitch Ball Grid Array
FC	Flip Chip
FPC	Flexible Printed Circuit
FEM	Finite Element Model

G

GPS	Global Positioning System

H

HDI	High-density Integration

I

IC	Integrated Circuit

I/O	Input/output
IBM	International Business Machines
IMB	Integrated Module Board
IR	Infrared
IMEC	Interuniversity Microelectronics Center

K

KGD	Known Good Dies
KPI	Key Performance Indicator

L

LSI	Large Scale Integration
LIFT	Laser-Induced Forward Transfer

M

MEMS	Micro-electro-mechanical systems
MCM	Multi-Chip-Module
MSL	Moisture Sensitivity Level

N

Nd-YAG	Neodymium-doped Yttrium Aluminum Garnet

P

PoP	Package-on-Package
PDA	Personal Digital Assistant
PCB	Printed Circuit Board

PI	Polyimide
PDPI	Photo-definable Polyimide
PTH	Plated Through Hole
PTCE	Packaging Test Chip version E
PTCL	Packaging Test Chip version L

R

RF	Radio Frequency
RPS	Rotations Per Second
RPM	Rotations Per Minute
RIE	Reactive Ion Etching
RT	Room Temperature
RCC	Resin Coated Copper

S

SMT	Surface Mount Technology
SMD	Surface Mount Device
SHIFT	Smart High-Integration Flex Technologies
SEM	Scanning Electron Microscope
sccm	standard cubic centimeters per minute

T

TC	Thermal Cycling
TMV	Through Mold Via
TSV	Through Silicon Via
THV	Through Hole Via
TH	Through Hole
TIPS	Thin Interconnected Package Stacks

U

UTCP	Ultra-Thin Chip Package
UTC	Ultra-Thin Chip
UV	Ultra-Violet
USA	Ultrasonic agitation

V

via	vertical interconnect access
VIP	Vertical Interconnect Pillar

X

X-ray CT	X-ray Computed Tomography

List of Symbols

E	Laser Power
f	Pulse repetition rate
d	Spot size of YAG laser
n_1	Pulses at a place
n_2	Number of places per round
n_3	Pulses per round
n_4	Total pulses at a place
n_5	Total round
N	Total pulses to drill one THV
R	Round per sec
D	Through Hole diameter
Φ	Laser fluence
Φ_{eff}	Effective fluence
CTE_i	CTE of individual material
Y_i	Young's modulus of elasticity of individual material
V_i	Volume of individual material
CTE_{eff}	Effective CTE of the composite

L	Linear dimension of the package
ΔL	Change in package dimension after release from carrier
ΔT	Difference between PI curing temperature and room temperature
ΔCTE	Difference between effective CTE of the package and the carrier
η_{eff}	Effective yield of stacked UTCP process
η	UTCP process yield
n	Number of UTCP sheets for PoP assembly
η_u	Stack yield derived from PoP assembly of multiple UTCP sheets
η_s	Yield of stacking process
T	Transmittance of a material with fixed wavelength of radiation
α	Attenuation coefficient of a material
t	Thickness of the material

Summary

The semiconductor industry strives to encompass "More-than-Moore" solutions for future electronic systems. On the same platform, microelectronic technologies that enable high density integration (HDI) of integrated circuits (IC) are becoming increasingly important. IC integration is traditionally done using two-dimensional (2D) approaches where the active and passive components are assembled on a rigid substrate. However this 2D integration approach fails to meet the HDI-requirements of current generation's smart electronic devices. In order to meet with the need for increased compactness in electronic packages, vertical integration is proven to be essential. As a result, the focus of most industries targets the transition of 2D- to 3D-integration, which replaces the surface level integration of multiple electronic components by employing the z-axis as the 3rd dimension of interconnection. Package-on-Package (PoP) and Through Silicon Via (TSV) are the known 3D-integration concepts, being adopted in many research groups and various industrial processes.

In Package-on-Package (PoP) techniques, the benefits of traditional packaging are combined with those of die-stacking techniques. Traditional packaging places each die in its own package designed for PCB assembly. The Die-Stacking technique stacks multiple packages in vertical direction forming a single stacked package. In traditional PoP configurations, the interconnection is made either by wire-bonding or ball grid array (BGA) at the edge of the package and/or chip. Both the techniques slightly increase the length and width of the package and usually require an extra interposer layer or under-filling material between the packages and/or chips. Through-silicon vias (TSVs) technology has the advantage of replacing edge wiring and/or BGA by creating vertical connections through the body of the chips. However, TSV introduces an added risk of damaging the active surface of the chips while creating the vias.

The Ultra-thin chip package (UTCP) technology is a thin-film based packaging technology where a fan-out metallization is used to redistribute the I/Os of the IC. It has the capability of producing thin and flexible electronic packages which can easily be embedded inside commercially available flexible circuit boards (FCB). It can be integrated with the circuit components by use of through hole via (THV) technology where the vias are made on the fan-out contact pads of the package, as opposed to vias through the chip as used in TSV technology.

By combining the concept of UTCP with traditional PoP and TSV technologies, a new 3D-stacking technology is created which targets a broad field of industrial and medical

electronic applications. In this PhD research work, a HDI technology is developed which is based on the aforementioned three technologies. The development principles and fabrication processes are the topics, discussed in this dissertation. A brief overview on IC packaging trends as per today's demand is summarized in Chapter 1. This includes the pros and cons of some of the available HDI technologies. The last part of this chapter covers the state-of-the-art of the new 3D-stacking concept for producing miniaturized multi-chip-modules.

Chapter 2 contains the 3D-stacking principle based on UTCPs which was developed during the initial phase of the PhD. The UTCPs are fabricated by embedding $\sim 30\mu m$ thick chips within two spin-on polyimide (PI) layers forming a flexible package of total thickness $\sim 60\mu m$. Connection to the outer world is made by fan-out metallization from the contact pads of the chip. These thin and flexible packages are next 3D-stacked using a vacuum lamination process, after leveling each package via layer-to-layer alignment. A non-conductive thin film adhesive is used as bonding material in between vertically leveled packages. 3D-interconnection is made by making Through-Hole Vias (THVs) on the stacked fan-out contact pads of the package. The specific properties of each material used in the stacking process are discussed in this chapter, as well as the reporting of the process development, such as the lamination parameter optimization towards a uniform adhesive layer within the stack. The THV technology also makes use of laser ablation micromachining for making THVs, followed by metallisation using electroless and galvanic copper plating. The laser ablation parameters are optimized to get smooth TH wall with less adhesive melt and/ or undercutting problem.

Chapter 3 describes the realisation and making of a stacked demonstrator, which consists of a stack of four EEPROM die UTCPs, having an application in Hearing Aid Device manufacturing. The stack is designed in such a way that the memory capacity of each stacked module is increased by four within the geometrical space of a single EEPROM die. To make the UTCP production cost effective, multiple packages are fabricated in large scale on a single substrate. For making a stack of four packages as the end product, the packages with different layouts are processed on separate substrates. After completing the packaging process, all the panels containing multiple UTCPs are released from the rigid carrier, aligned and stacked vertically by vacuum lamination process. THV process enables making the interconnection between the vertically stacked packages. Top and bottom side patterning of the copper and singulating each of the stack completes the fabrication process. Functionality of UTCPs can be verified before the stacking process which opens the possibility of estimating and improving the yield of the full stack. However, the yield of the stacking process was found to be significantly smaller than the calculated value. The failure analysis of the stack shows that topographical difference at the chip edge of the thin package leads to thin die cracking. Applied pressure during the lamination process plays an important role at the non-flat edge of the conventional UTCP. Non-uniformity in applied pressure at this region is the reason behind this die cracking problem. This analysis shows the direction of further development in this technology. It includes yield improvement of multiple-UTCPs by using a proper thin-die bonding technology as well as the development of a Flat-UTCP technology for improving the yield of the stacking process.

Chapter 4 describes the Flat-UTCP concept and development process. In this concept

an extra PI layer is introduced, having the same thickness as the Ultra-thin Chip (UTC). In order to make the whole package flat at the chip edge, it is necessary to create a cavity in this polyimide layer, having the dimensions of the chip. The use of negatively toned photodefinable polyimides (PDPI) makes the cavity process straightforward, by using the previously bonded thin chip as a mask, thus creating a self-aligned cavity. The vias to the chip are conventionally drilled using laser ablation technology. However this approach has the unavoidable risk of damaging the contact pads of the chip. Also the beam-shaping optics of the laser needs a regular calibration for getting a reproducible via shape. A PDPI based photo-via process eliminated all these risks linked to the laser ablation process. To reduce the processing cost, it is necessary to produce these Flat-UTCPs on a large scale. Selecting a correct set of materials for the large area process is discussed in the first part of this chapter. It is then followed by basic fabrication issues related to CTE mismatch between carrier-PDPI layer which results in package deformation after UTCP release and precise bonding of multiple UTC on the PDPI substrate. A redesigned process flow to reduce the degree of deformation by introduction of stress-relief grooves in the PDPI layer is discussed in this chapter. Precise placement and bonding of thin chips by use of BCB as glue material is described in details.

Chapter 5 gives the detailed fabrication process of the EEPROM prototype based on Flat-UTCP concept. As per the failure analysis given in Chapter 3, the package distribution per panel plays a role in lowering the yield figure of the stacking process. This has been addressed and a rotational symmetry in package distribution per panel is introduced in the package design. The stacking process yield in this particular case by using Flat-UTCPs has found to be 83% which is much higher as compared to that in conventional UTCP stacking process (15%). However, an increase in total stack thickness from $300\mu m$ to $360\mu m$ is noticed by stacking 4 Flat-UTCPs, each embedding $20\mu m$ thick EEPROM dies.

Chapter 6 gives an overview on the further development activities which have been initiated in the frame-work of the PhD. This includes a laser-assisted package release process to replace the salt-based release process, which has shown yield risks during wet processing. Also thermo-mechanical behavior of these thin stacks is an important factor to be studied. A brief discussion on the circuit design and thermal measurements by using a dedicated thermal test chip (PTCL) is described in the last part of this chapter.

Samenvatting

De halfgeleider-industrie neigt naar het gebruik van More-than-Moore-technieken voor microsystemen. Hierbij wordt gezocht naar proces-technologieën die toelaten om verscheidene geïntegreerde schakelingen (IC) op compacte wijze op hetzelfde substraat te integreren, waarbij de densiteit van de interconnecties drastisch toeneemt (High Density Integration of HDI). In de conventionele aanpak voor het integreren van ICs worden de actieve en passieve componenten naast elkaar op hetzelfde harde substraat geplaatst. Deze 2D-aanpak voldoet echter niet meer aan de eisen voor hoge-densiteitsintegratie die gesteld worden door de huidige generatie elektronica. De oplossing wordt gevonden in het gebruik van de derde dimensie door middel van verticale integratie. Twee bekende concepten voor 3D-integratie die vandaag door de industrie en in onderzoek gebruikt worden zijn Package-on-Package (PoP) en Through-Silicon-Via (TSV).

In de eerstgenoemde Package-on-package (PoP) aanpak, worden de voordelen van traditionele chip-verpakkingstechnologieën gecombineerd met die van chip-stapeltechnieken (die-stacking). In de traditionele technologie worden de ICs één voor één verpakt voor verdere PCB-assemblage. De chip-stapeltechnieken combineren dan weer verscheidene ICs boven elkaar tot één module, dewelke als verpakking kan gebruikt worden. In de PoP-technologie worden verscheidene van dergelijke ICs en verpakkingen gecombineerd, en met elkaar verbonden door miniscule draadjes (wire-bonding) of door middel van een matrix van soldeer-balletjes (ball-grid array of BGA). Hierdoor stijgt het gebruikte oppervlak van de verpakking lichtjes, en vaak is een extra tussen-substraat (interposer) of vullende lijmlaag (underfill) nodig.

De techniek van Through-Silicon-Vias (TSV) vermijdt deze fijne bekabeling met zogeheten wire bonds, of de BGA, door verticale verbindingen te maken doorheen het silicium van de IC. Hierbij neemt dan wel het risico op schade aan de actieve oppervlaktelagen van de IC toe.

De ``Ultra-Thin Chip Package"-technologie (UTCP-technologie) is een dunne-film gebaseerde chipverpakkingstechnologie waarbij een uitwaaierende metallisatielaag gebruikt wordt om de hoge densiteit van interconnecties op de chip uit te spreiden tot een lagere densiteit, die compatibel is met de mogelijkheden van conventionele 2D-integratie. Deze dunne en flexibele chip-verpakkingen kunnen ook ingebed worden in commercieel beschikbare flexibele substraten (FCBs), waarbij de verbindingen met de IC gerealiseerd worden door middel van gemetalliseerde vias naar de uitgewaaierde contacten op de UTCP.

Door de technieken van UTCP-verpakkingen te combineren met de PoP- en TSV-technologieën ontstaat een nieuwe 3D-verpakkingsstrategie die toepassingen vindt in een breed gamma van elektronica voor industriële en medische doeleinden. In dit doctoraatsonderzoek werd deze hoge densiteits-verpakkingstechniek ontwikkeld, gestoeld op de eerder vermelde technieken. Dit manuscript verhaalt het ontwikkelen ervan en beschrijft het proces, de productiemethode en zijn toepassingen. Een kort overzicht van de huidige trends in IC-verpakkingstechnologie, met hun voor- en nadelen, wordt beschreven in hoofdstuk 1. Dit hoofdstuk sluit af met de stand van zaken wat betreft 3D-verpakkingstechnologie voor het maken van multi-chip modules.

Hoofdstuk 2 beschrijft de basisprincipes van het opeenstapelen van UTCPs, zoals die tijdens de eerste fase van het doctoraatsonderzoek geconcipieerd werden. De UTCP-verpakkingen bestaan hier uit een dunne chip met een dikte van slechts $\sim 30\mu m$, ingebed tussen twee polyimide lagen. Op deze wijze wordt een flexibele verpakking met een totale dikte van $\sim 60\mu m$ bekomen. De elektrische verbinding tussen de chip en het systeem wordt verzekerd door een dunne-film metallisatie, dewelke de hoge densiteit van de contactpaden uitwaaiert tot een lagere densiteit. Deze dunne verpakkingen worden vervolgens opeengestapeld met behulp van vacuüm-laminatie techieken, nadat de individuele verpakkingen werden opgelijnd. De verticale interconnecties (3D) worden verzekerd met behulp van Through-Hole Vias (THVs). In dit hoofdstuk worden de materiaalparameters van de gebruikte materialen besproken, en er wordt ook dieper ingegaan op de ontwikkeling van het proces. Zo wordt er gebruik gemaakt van laser ablatie voor het realiseren van de THVs, gevolgd door een metallisatiestap met behulp van zowel electroless als galvanisch opplaten van koper. De parameters voor deze laser ablatie werden geoptimaliseerd naar gladde via-wanden toe, waarbij de fenomenen van *melt* en *undercutting* geminimaliseerd werden.

Hoofdstuk 3 beschrijft de realisatie van een prototype bestaande uit een *stack* van vier EEPROM geheugenchips, verpakt in een UTCP, die zijn nut bewijst in het ontwerp van hoorapparaten. De *stack* realiseert op die manier de performantie van vier ICs binnen het geometrische volume van één chip. Om de kosten van de UTCP productie onder controle te houden worden de verschillende lagen van de *stack* afzonderlijk geproduceerd. Eens de individuele lagen afgewerkt zijn, worden de flexibele substraten losgemaakt van hun tijdelijke drager, en na oplijnen met elkaar verlijmd door middel van vacuüm-laminatie technieken.

Het THV-process wordt dan toegepast om de lagen elektrisch met elkaar te verbinden. Tot slot worden de koperpatronen aangebracht op de boven- en onderlagen. Vooraleer de individuele lagen verenigd worden kan de functionaliteit van elke UTCP afzonderlijk getest worden. Dit laat toe om een controle uit te voeren op de *yield* van het totale proces, inclusief de verlijming van de lagen. Hier werd aangetoond dat de uiteindelijke *yield* van het verlijmen te laag lag. Een analyse van de falingsmechanismen toont aan dat de oorzaak kan gevonden worden in de topografie aan de rand van de IC, waar barsten in het silicium worden waargenomen. Deze zijn het gevolg van een niet-uniforme drukverdeling tijdens laminatie. Deze vaststellingen hebben geleid tot de verdere ontwikkelingen dewelke in de volgende hoofdstukken besproken worden, teneinde de *yield* onder controle te houden, onder meer door een geoptimaliseerd verlijmproces enerzijds, en het ontwikkelen van een topografisch vlakke UTCP

anderzijds.
In hoofdstuk 4 wordt dieper ingegaan op het begrip *Flat UTCP* en de ontwikkeling ervan. Hierbij wordt een extra laag polyimide aan het basisproces toegevoegd, waarvan de dikte die van de chip evenaart. Om de topografie vervolgens weg te werken, wordt een caviteit rond de IC gemaakt. Dankzij het gebruik van een lichtgevoelige variant van het polyimide (*PhotoDefinable Polyimide* of *PDPI*) kan dit eenvoudigweg gerealiseerd worden door de IC zelf als definitiemasker te gebruiken voor de caviteit, waardoor beiden nauw bij elkaar aansluiten. Bovenop deze caviteit komt tot slot de polyimidelaag waarin de vias worden gedefinieerd. De mogelijke schade die het gevolg kan zijn van het laser ablatieproces dat gebruikt wordt voor de via-definitie kan hier vermeden worden door opnieuw gebruik te maken van het fotogevoelige polyimide (PDPI). Tot slot wordt opnieuw dieper ingegaan op de materiaalkeuzes bij de realisatie van deze UTCP verpakkingen. Zo resulteert een verschil in de thermische eigenschappen van het polyimide en het processubstraat in een vervorming van de vrijstaande UTCP-verpakking. Hier wordt dieper op ingegaan. Ook de keuze voor BCB als bindmiddel tussen de IC en het polyimide wordt toegelicht.
Hoofdstuk 5 verhaalt de productie van de EEPROM demonstrator met behulp van het *Flat UTCP*-idee. Zoals in de *yield*-analyse van hoofdstuk 3 werd aangetoond, heeft de plaatsing van de ontwerpen op de verschillende lagen van de *stack* een effect op de uiteindelijke *yield* van het proces. Hiervoor werd een techniek uitgedacht waarbij de verschillende lagen in een ontwerp worden ingewerkt met behulp van een rotationele symmetrie. De resulterende *yield* van alle toegepaste verbeteringen bedroeg 83%, wat een significante verbetering inhoudt ten opzichte van de eerder opgemeten 15%. Deze verbetering gaat echter ten koste van een kleine toename van de totale dikte van $300\mu m$ tot $360\mu m$, waarin vier EEPROM chips verpakt zijn.
Tot slot wordt in Hoofdstuk 6 een overzicht gegeven van de lopende ontwikkelingen die hun oorsprong vinden in dit doctoraatswerk. Hier wordt onder andere gewerkt op het gebruik van laser-technieken voor het losmaken van de UTCPs van de tijdelijke substraten. Een tweede onderzoeksgebied handelt over het thermo-mechanische gedrag van een *stack*. Hiertoe werd een test-circuit ontworpen gebaseerd op een daartoe ontworpen thermische test chip.

Chapter 1

Introduction

1.1 System Miniaturization Trend

An emerging trend in electronic systems is referred as "convergent systems" by Rao et al. [1]. It is characterized by the convergence of computer, communications, consumer, and biomedical product functions into one product. High Density Integration (HDI) has a critical role in next-generation convergent systems which at the end leads to "system miniaturization". It has two major components: (a) Integrated Circuit (IC) packaging which enables in connecting microscopic IC world to macroscopic outside world, and (b) System packaging which involves multiple levels of packaging and primarily driven by discrete packaging of IC's and components [2].

Examples of the next-generation convergent systems include electronic products such as smart watches with cell phone, global positioning system (GPS), sensor and web mail access, and medical electronics such as smart medical implants with computing, sensing, imaging, and wireless communication characteristics, as illustrated in Figure 1.1. The technologies required to accomplish this convergence of data, video, voice, sensing, and other functions are digital, optical, RF, analog, MEMS, and sensors [1].

1.2 IC Packaging Trend

The rapid evolution in microelectronic technology has remarkable role in system miniaturization. It enables the integration of a huge number of transistors on a given area of silicon with decreasing feature sizes on ICs. This results in size reduction and increased complexity in design of the basic unit cells in memory and logic devices. This increase in complexity is measured by the number of transistors integrated on a single die and is characterized by "Moore's Law".

High performance of a device demands the circuits to run at higher speeds. Generally, the clock speed at the off-chip are much lower than on-chip, largely due to limitation in the interconnect technology. It is therefore of importance to improve the electrical

performance of IC packages and interconnect technologies. Because of the finite speed of electrical signals, this also implies a strong miniaturization of the high frequency system, e.g. placing die closely together on a single high density interconnection substrate (Multi-Chip-Modules, MCM) [3]. The impact of the microelectronic technology trends on the IC package and interconnection technology are summarized below in Table 1.1.

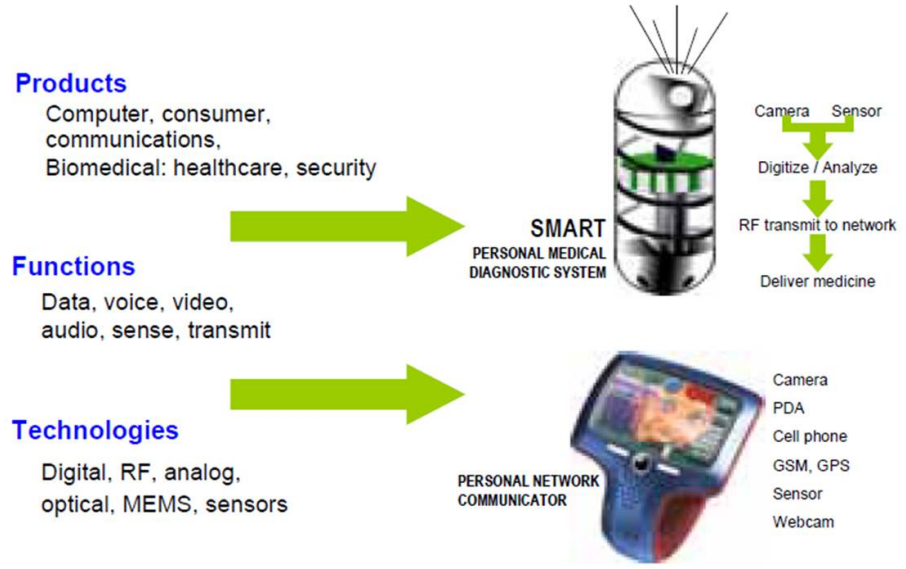


Figure 1.1: Trend to convergent and miniaturized systems such as smart watches and smart implants [1]

IC integration has traditionally been done using two-dimensional (2D) approaches. In today's expanding and demanding electronic consumer market, 2D-integration has shown serious limitations when it comes to computing, wireless and wired communication systems [4]. In order to achieve compact packages with more efficiency, vertical integration approach have been proven to be essential. And this approach motivates most of industries to look into the trend of transition from 2D- to 3D-integration technologies [5], [6]. Figure 1.2 shows the emerging technology platforms in this direction of development. This includes Package-on-Package, Package-in-Package, Wire bonded Chip stack, Through Silicon Via stacking, etc. All these concepts have their own advantages which make them suitable for some applications and also disadvantages which need development by adopting new technology platform. In the following sections, a brief discussion on some of the recent 3D-integration technologies are given. The evolution of a novel HDI concept based on all these concepts is described in the last section.

Table 1.1: Summarized Package requirement corresponding to IC trend [3]

IC trend	Package requirement
More I/O's with higher density	• High Density wire bond or flip chip techniques • Reduction in the package size by reducing pin pitches and the use of area array connection • Higher interconnect density interconnection boards to handle the higher I/O density on the packages
Larger IC area	• Thermo-mechanical reliability concern: Requirement of reduction in mechanical stress on die and package joints
Higher speed	• Low package parasitics (inductance, coupling) • High density packaging to reduce interconnection delays • Low dielectric constant materials
High power dissipation	• Low thermal resistance in the IC-packaging • Improved system-level cooling concepts required

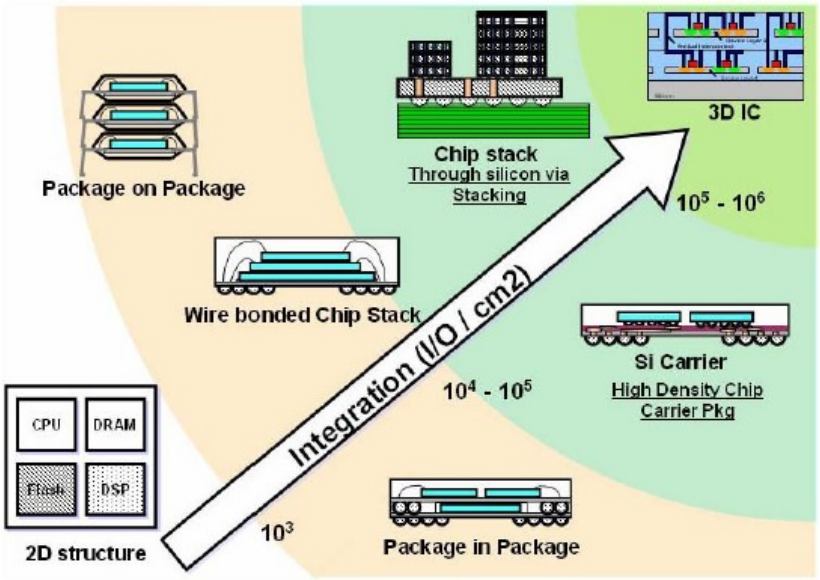


Figure 1.2: Emerging 3D silicon integration[7]

1.2.1 Package-on-Package (PoP)

Package-on-Package (PoP) is an IC packaging technology which allows vertical integration of discrete IC's or packages with embedded IC's. In traditional PoP design, the top package is a stacked-die memory product and the bottom package contains a logic processor. The perimeter area of the top surface of the bottom package typically has Fine-pitch Ball Grid Array (FBGA) land pads. The solder balls on the bottom surface of the top package substrate are soldered on the BGA land pads located on the top surface of the bottom package substrate. The solder joints provide z-axis interconnection for the logic device mounted on the top surface of the bottom package. A typical example of the PoP stack is given in Figure 1.3. It has become an attractive solution for high-density package used in various products such as mobile phone, PDA and digital camera [8], [9]. PoP components were presented in 2003 by Nokia (Finland) and Amkor (USA, Arizona) as a result of a cooperative development [10]. In 2007 many companies started utilizing the PoP technology in their advance designs.

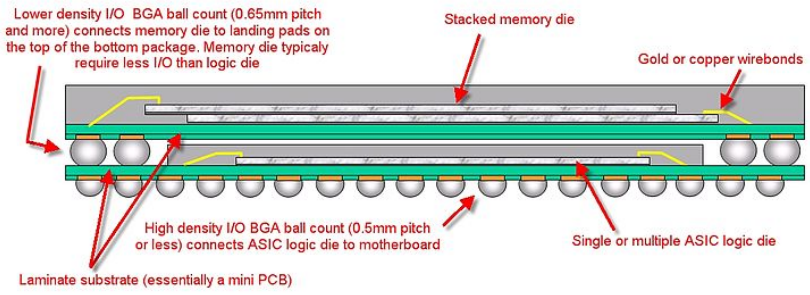


Figure 1.3: Typical logic plus memory PoP stack, common to mobile phone application processors or base band modems from 2005 onward [11]

The benefits of PoP design are motherboard space saving [11], a mix and match logic with multiple memories, flexible combination and assembly [12]. Electrically, PoP offers benefits by minimizing track length between different inter-operating parts. This yields better electrical performance of devices with reduced noise and cross-talk. The packages can be tested separately before making the final assembly. This is having advantage over stacked-die packages where the entire set is useless where there is no scope of choosing "known good" ones.

Together with all these essential benefits, PoP has also some issues related to mechanical stability at high temperature processes. The disconnection between the solder balls (z-axis interconnection) at a high reflow temperature is one of these issues [13], [14]. This is mainly because of the warpage in the top and bottom packages in the opposite direction. A developed package structure by ASTRI (Figure 1.4) deals with this issue in traditional PoP design. It includes FBGA format for both top and bottom packages, large stand-off height for die stacking in the bottom package and low warpage behavior

of the bottom package with mechanically balanced package structure [15].

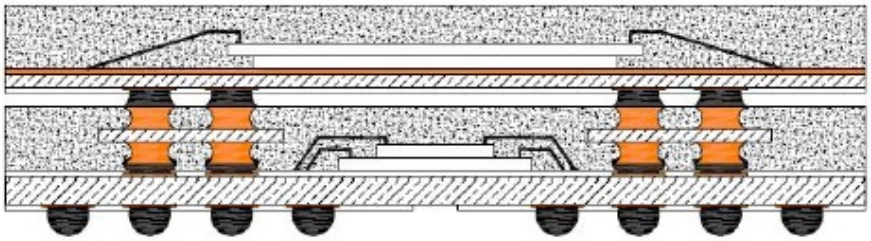


Figure 1.4: PoP structure by ASTRI: FBGA format for both top and bottom packages, large stand-off height for die stacking in the bottom package and low warpage behavior of the bottom package [15]

Use of under-filling material between the packages can improve mechanical stability of the solder joints [16]. The underfill material is dispensed or jet printed directly next to the packages. The material is drawn in between the bumps by capillary forces.

Amkor's Through Mold Via (TMV) method (Figure 1.5) uses laser processed via constructions through the bottom package. The vias expose the stacking interface pads on the top metal layer of the interposer and is then filled with conductive material to form a stacking interface for the top package. The bumps of the top package are connected to these interfaces and joints are formed after the soldering process step. This method enables dense routing with reduced warpage in the package [17].

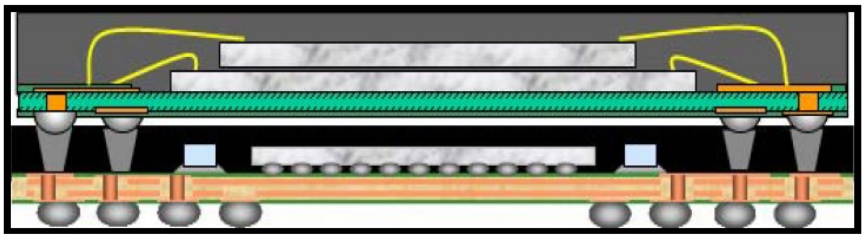


Figure 1.5: PoP structure by Amkor: Through Mold Via technology enables dense routing with reduced warpage in bottom package [17]

Future applications demands PoP base package with increased interconnect density, reduced pitch, reduced package size and thickness with improved warpage control. Reduced tooling cost and capability to handle various interconnect configurations will make this technology more versatile. To deal with some of these issues or demands,

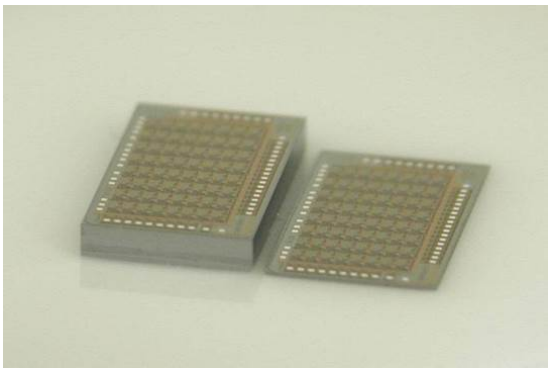
a thin package stacking approach is developed in the frame work of European Union FP7 Project TIPS (Thin Interconnected Package Stacks). The whole process includes fabrication of Ultra-Thin packages for electronic components followed by PoP stacking by lamination eliminating the need of under-filling and related issues. A brief overview of this thin packaging technology is given in the next section.

1.2.2 Ultra-Thin Chip Package (UTCP)

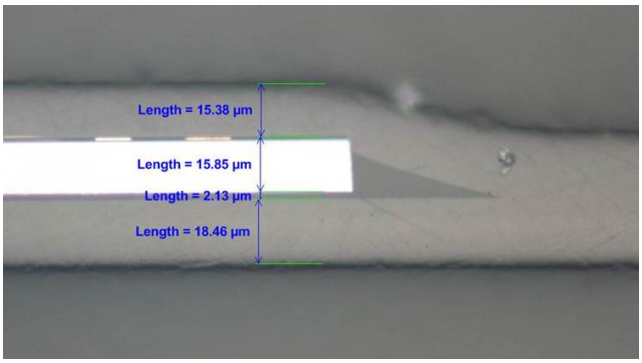
This is a thin film based packaging technology where the dies are thinned down to $\sim 20\mu m$ and embedded in spin-on polyimide materials with face-up die bonding on the base polyimide (PI) surface. An electronic circuit can be made on the covering PI layer after making interconnections to the chip, which is completely encapsulated within the PI layers. Primarily this was done by making vias on the contact pads of the thin chip by laser processing [18] on the covering PI layer. Later on a photo-via technology was introduced [19] by use of photodefinable polyimide (PDPI) as the base and covering PI layer. This is then followed by thin film processing for metal routing which enables fan-out wiring from the contact pad of the chip to the off-chip area. This results in formation of ultra-thin and flexible package of approximate thickness $50\mu m$. This technology is being developed by many of the researchers in last decade by our CMST research group [20], [21]. An example of 2 PI-layered UTCP cross-section is shown in Figure 1.6.

UTCPs are based on PI material, thinned chips and thin film metal interconnects. All these layers are so thin that they can be easily bendable without damaging the active components. This mechanical robustness makes it a good candidate to integrate it inside commercially available Printed/ Flexible Circuit Boards (PCB/ FCB). Dies with small bond pad and pitch size are difficult to align while integrating them directly in the PCBs. The fan-out metalization gives a flexibility in broadening the pad and pitch sizes at the off-chip area. As a result, the typical pitch size of the dies, which is of the order $100\mu m$, can be easily aligned and integrated within the FCBs with having pitch of dimension $1mm$. Another advantage of this fan-out metalization is that it enables easy testing of the packages on the broader contact pads. This in turn makes the easy selection of "Known Good" packages before assembling them inside the system or device. The concept of integrating UTCPs in FCBs has been proven in 2009 [22].

Like the traditional PoP concept, the individual UTCPs can also be aligned and 3D-stacked in a well-defined pattern. This makes the whole module compact in size with eliminating the issues related to mechanical stability in conventional PoP. Unlike PoP where the z-axis connection is made by BGA at the periphery of the chip packages, here it can be made by Through Hole Via (THV) at the fan-out contact pads of the packages. The concept of THV is extracted from the Through-Silicon Via (TSV) which is one of the 3D-integration technologies. A brief introduction to this TSV and other developing interconnection technologies is given in next section.



(a)



(b)

Figure 1.6: UTCP technology based on the conventional principle of 2-layered PI (a) Silicon Chip thinning to the order $15 - 20\mu m$, (b) Cross-section of the thin package with a thickness of order $40 - 50\mu m$

1.2.3 Through Silicon Via (TSV)

Through Silicon Via (TSV) technology is a Vertical Interconnect Access (via) passing completely through a silicon wafer or die [23]. TSV is a high performance technique used to create 3D-packages and 3D-integrated circuits as an alternative to technologies such as PoP. The density of the vias is substantially higher and the length of the connections is shorter. In most 3D-packages, the stacked chips are wired together along their edges. Examples of the wire bonding can be seen in the schematics of different generations of PoP (Figure 1.3, 1.4, 1.5). This edge wiring slightly increases the length and width of the package and usually requires an extra interposer layer between the chips. TSVs replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D-package can also be more flat than an edge-wired 3D-package.

An alternate type of 3D-package can be found in IBM's silicon carrier packaging technology, where the IC's are not stacked but a carrier substrate containing TSV's is used to connect multiple IC's together in a package. The adoption of TSV is expected to be more performance and functionality driven. By using shorter connections in a three dimensional packaging, a faster signal transmission, higher clock rates and lower power dissipation can be obtained [4]. An example of such TSV structure in new 3D TSV Packaging Roadmap of Samsung is shown in Figure 1.7.

Together with 3D TSV, there is also another coexisting interconnection technology, Vertical Interconnect Pillar (VIP) which is based on Aerosel Jet Printing process [24]–[26]. Conductive polymer are used as 3D-interconnects which allows formation of fine conductive lines of width $30\mu m$ on 4 die stack and $100\mu m$ on 8 die stack, having a pitch of $200\mu m$ [26]. An example of this VIP connection on a 8 die stack is shown in Figure 1.8.

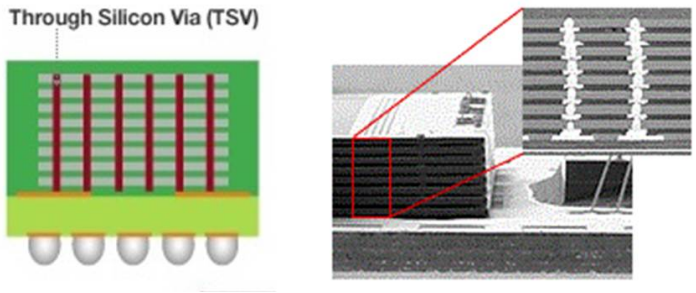
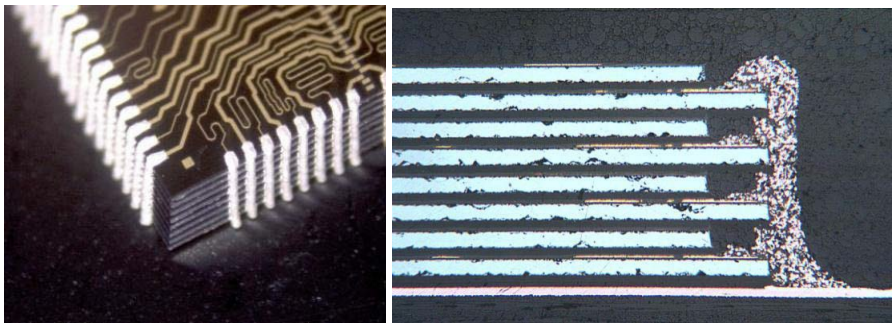


Figure 1.7: Cross-sectional microstructure of 3D TSV micro-joints [27]



(a) (b)

Figure 1.8: Vertical Interconnect Pillar (VIP) technology interconnecting an 8 die memory stack (a) tilted view, (b) cross-sectional view (source: Vertical Circuits Inc. [26])

1.3 State-of-the-Art

Using the basic concepts of the above said 3 technologies, a new module miniaturization concept is developed and discussed in this dissertation. *Ultra-Thin Chip package (UTCP)* is the core technology which drives the development of the entire process. It is one of the semiconductor packaging technologies which is completely based on thin film technology. Like most of the thin film processes, the UTCPs are fabricated on the glass carrier with various coating, deposition, lithography and material etching processes. As a result, the package will contain layers of 10's of micron thickness including the thinned chip. After fabrication process, they can be tested before release from the carrier. The thinness and flexibility of the package (including the embedded die) makes it a suitable candidate to use it in PCB industries as a flex material [21], [28]. By taking advantage of its thinned and almost flat structure, they can be 3D-staked by adopting both *PoP* and *TSV* technologies to construct a stack of minimized dimension.

The topography of individual package gives rise to the gap filling issue which is one of the disadvantages in conventional *PoP* technology. Use of under-fill material sometimes leaves a gap of $10 - 20\mu m$ [16]. The average thickness of the UTCPs is of the order of $50\mu m$ with almost negligible topographical offset as compared to the packages in PoP technology. In this process, a non-conductive thin film of adhesive layer can be used as interposer and/or glue material in between the vertically stacked flex of UTCPs. An example of 3D-stack of ultra thin packages with embedded silicon dies, produced by vacuum lamination is shown in Figure 1.9. Each of the UTCPs in the stack is of thickness $\sim 50\mu m$ (embedding chip of thickness $20\mu m$), giving rise to a stack of total thickness $\sim 360\mu m$.

As the UTCPs have metal fan-outs, after stacking it enables making *Through Holes Vias (THV)* in the outer contact pads of package. This is also named as Through Mold Vias (TMV) by some research groups working on similar concept [29], [30]. This THV is having advantages over the TSV in the processing aspect where the wafer handling and Laser drilling on active IC surface are critical factors in processing point of view. Active area of the chips is a dimensional constrain for TSV technology which leads to different failure mode. This includes the risks of potential failure due to Silicon depletion at and around via, and thermally induced stress which lead to crack formation in silicon dies [24], [31], [32]. In case of THV, the vias are made on the stacked metal fan-outs of the thin packages which is much more relaxed as compared to TSV (independent of active area dimension of the chip).

The technology development for lamination of packages and fabrication of such THV with TH plating process are given in Chapter 2. Figure 1.10 shows X-ray CT scan picture of a single stack containing 4 chip packages, including a total of 6 through hole interconnects. X-ray tomography is a nondestructive way for failure analysis and assembly analysis in the circuits. As the metal has higher opacity as compared to other materials in the stack, the available analysis technology at UGCT (Center for X-ray Tomography, Ghent University [33]) enables detection of only metal tracks.

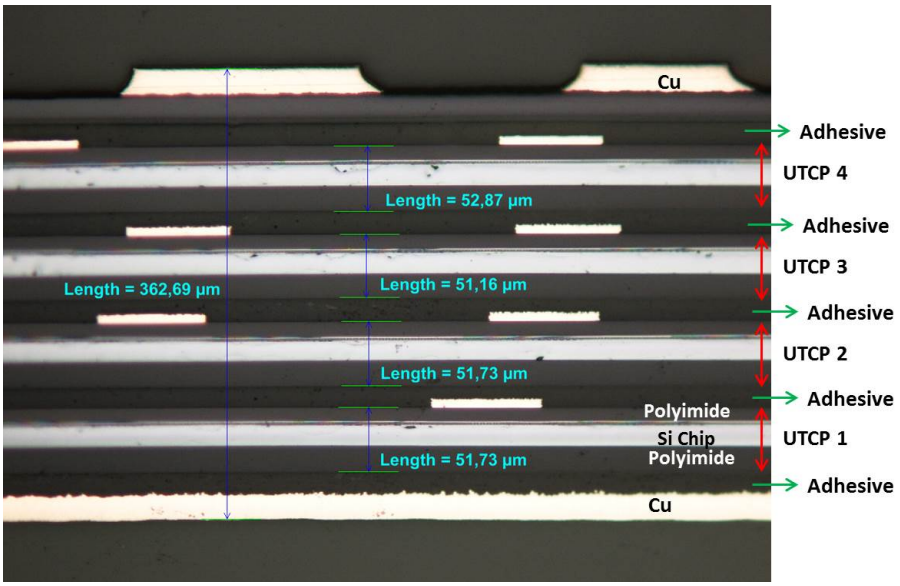


Figure 1.9: Cross-section of a 3D-stack fabricated by laminating 4 UTCPs

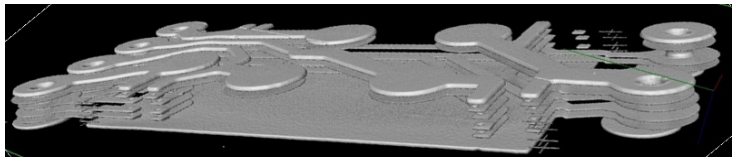


Figure 1.10: X-ray micrograph of 4 layered package stack including through hole interconnects: showing only metal circuits within the stack

1.4 Research Focus

As the whole technology is based on UTCP, it has advantages over some of the traditional 3D-integration technology where compactness is a point of concern. However, the fabrication process needs special attention when thin chips and CTE of different materials in the stack plays an important role. Some of the issues related to development of this concept are listed below.

1.4.1 Thin die cracking issue

The conventional UTCP process includes thin chips down to $20 - 30\mu m$ thickness which is embedded in two polyimide thin film layers each of thickness $\sim 20\mu m$. After placing the chip on the 1st polyimide layer, the 2nd layer is spin-coated over the entire

surface covering the thin chip. This results in a thickness offset at the chip edge of the package. Although the effect due to this thickness offset is not addressed when a single package containing Microcontroller is embedded in a flex circuit [22], it affects severely when multiple packages are stacked vertically. It induces thin die cracking within the stack which demands the entire package to be flat before laminating.

As an attempt to fabricate these UTCPs in industrial scale, the technology is transferred to a Swiss based flex company HighTec MC AG [34] in the frame work of TIPS project. The stack produced by laminating these conventional UTCPs, gave rise to loss in yield after stacking. In due time, it was observed that it is a consequence of the thickness offset at the chip edge of the conventional UTCPs which lead to thin die cracking. The entire mechanism of the lamination process in which this defect can be introduced in the stack is given in Chapter 3.

1.4.2 Low cost fabrication issues

Vacuum Lamination and THV are the low cost processing approach adopted in many PCB industries. To develop the whole technology for low cost production, the UTCP flexes have to be available commercially for 3D-stacking approach. This means large area production of packages embedding well-aligned thin chips. However face-up alignment and void-free bonding are the assembly issues due to fragile nature and warpage in thin chip [35], [36]. The consequences of these issues in UTCP technology are addressed in Chapter 4, 5.

1.4.3 CTE mismatch issue

Flat-UTCP technology enables the production of thin packages with more or less uniform topography around the chip edge. Deformation of a flexible package is another source of yield loss in the UTCP mass production process. The right selection of materials and symmetry in the layer-to-layer build-up can reduce the effect due to CTE mismatch. A detailed analysis of this phenomena is given in Chapter 4.

1.4.4 Stacking Process Yield

The entire process yield is depended on 3 factors: the package production yield, number of packages within a single stack and the stacking yield. A difference in package topography has a major influence in the stacking yield. Additionally by introduction of rotational symmetry in the package distribution makes it easy to eliminate the non-functional package from the stack. This rotation factor has a role in improving the overall process yield which has been described in Chapter 5.

1.5 Acknowledgments

This PhD research is being financially supported by FP7 European Project TIPS (Thin Interconnected Package Stacks), Ghent University and IMEC (Interuniversity

Microelectronics Centre).

Chapter 2

Technology Development for UTCP stacking

2.1 Introduction

The stacking technology based on Ultra-Thin Chip Packages (UTCPs) is discussed in this chapter. The first section is giving a brief overview of this concept which was developed during the initial phase of the PhD work. The basic process steps involve lamination of thin flexible packages and realizing interconnections within the stacked electronic packages. For each developement step, it is necessary to evaluate the quality of this step, e.g., layer-to-layer adhesion of thin layers in stack after lamination, via processing by laser drilling and metalization. The experimental analysis of some of these process steps are elaborated in this chapter.

2.2 3D-stacking of UTCP concept

This is one of the high density integration technologies using the vertical axis as mode of interconnection. To make the whole 3D-stacked module compact, the individual packages have to be as thin as possible. A spin-on polyimide based UTCP technology with fan-out metalization has the capability to produce thin and flexible packages which can be embedded inside a PCB [21], [28]. The UTCP thinness and fan-out metalization makes it a proper technology for very compact package-on-package (PoP) configurations, by laminating several UTCP packages with a sequential vertical alignment. A Through Hole Via (THV) technology is developed to make vertical interconnection to the fan-out metalization of the UTCPs within the stack.

The overview of process flow is given in Figure 2.1. The whole process for producing these packages is described in details in the section 2.4.1. After release from the rigid carrier, they can be aligned sequentially and laminated by vacuum lamination process. For package-to-package bonding, a dry film adhesive material is used which liquifies

at temperature of $120°C$ and act as bonding material between the polyimide based packages during the curing process. The THVs are drilled at the fan-out metal contact pads of the stacked packages by laser micro-machining. These THVs are plated afterwards by seed layer deposition using copper electroless plating, followed by Copper thickening with galvanic plating process. As the final processing step, the copper is patterned by laminating dry film resist which protects the Plated Through Holes (PTHs) during Cu etching. The materials and technology used for this process are described in details in the following sections.

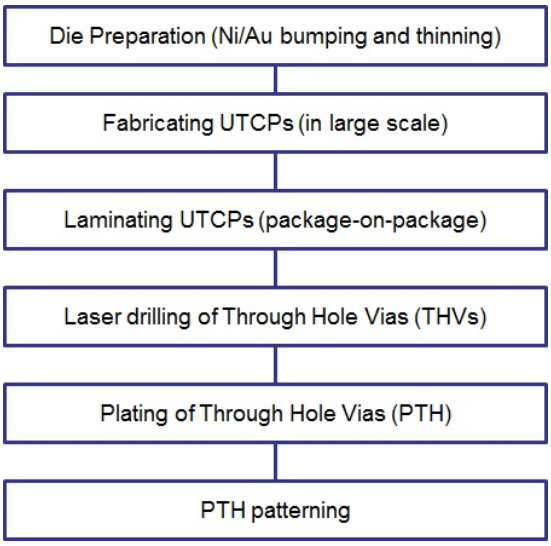


Figure 2.1: Process flow for developing UTCP stacking technology

2.3 Materials for UTCP Stacking

The basic materials for the stacked package fabrication are the thin chip packages, adhesive material for package-to-package bonding and the top and bottom side covering flexes for the stack. The properties of these materials are discussed in the following sections.

2.3.1 Ultra-Thin Chip Package

Fabricating UTCPs in industrial scale needs some changes in the conventional process flow. In the demonstrator production phase (Chapter 3), these changes are addressed. However, the materials used for the whole process are almost the same and are discussed below.

Diced Thin Chip

In several emerging applications, minimum chip thickness with chip flexibility are enabling requirements. UTCP technology is one of them and needs the dies to be thinned down upto the active region. Due to the thinness upto couple of micron level, they are named as Ultra-Thin Chip (UTC).Ultra-thin chip technology has potential to provide solutions for overcoming bottlenecks in silicon technology and for leading to new applications. Figure 2.2 illustrates various applications of these ultra thin chips.

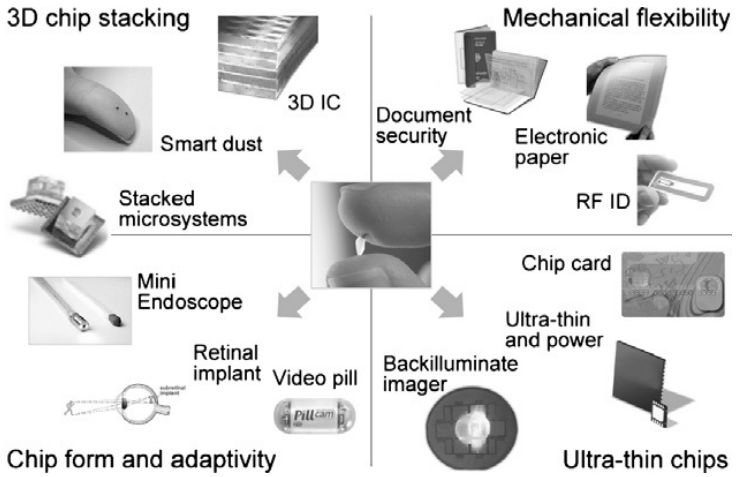


Figure 2.2: Target applications of ultra-thin chips[37]

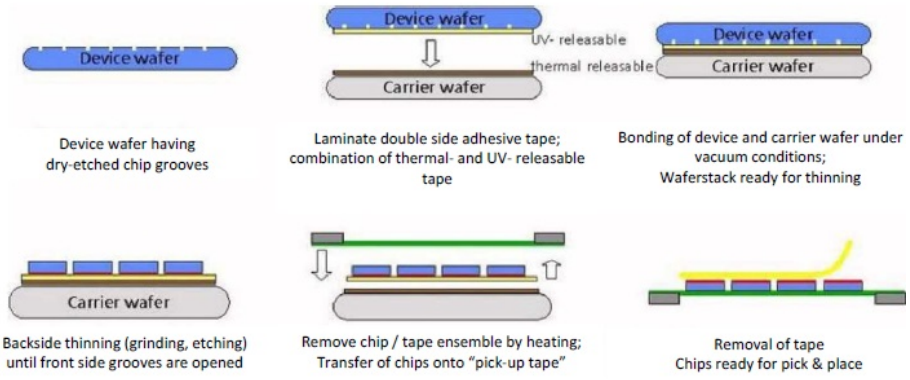


Figure 2.3: Schematic overview of the "dicing by thinning" principle followed by the transfer of the dies from the thinning carrier wafer to a low tack tape (source:IZM)

The commercially available ultra-thin diced dies are based on the principle of "Dicing by Thinning" [38]. The dicing of ultra thin wafers with standard sawing technologies has offered a range of challenges and problems in the past. To eliminate the influence of micro-cracks induced by sawing wafers, the Fraunhofer-Institute for Reliability and Micro integration developed this new concept of wafer dicing. Figure 2.3 shows the principle of the "Dicing by thinning" process. The concept allows manufacturing of upto $20\mu m$ thin wafers and includes self acting die separation during the thinning procedure. The process separates the thin and flexible integrated chips by defining a plurality of grooves into the front surface of the wafer to be thinned. The wafer will be thinned until the grooves are exposed. The grooves isolate each IC chip into a separate die.

Polyimide

Polyimide is thermo-setting resin durable in high temperatures, friction, radiation, and various chemicals. The base material for the conventional UTCP production is a spin-on polyimide. PI2611 from HD Microsystems, Parlin, NJ. [39] is suitable for this application because of its excellent mechanical and thermal properties. During the UTCP processing, materials are cured up to $350°C$ and high thermal stresses cannot be avoided during curing cycles. The coefficient of thermal expansion (CTE) of cured PI2611 film is $3ppm/°C$ which is very close to the CTE of silicon. This CTE match is important in order to prevent thermal stresses in the very thin silicon devices.

Later on a development in UTCP technology was reported by use of photodefinable polyimide (PDPI HD4110 [40]) with different fabrication concept. This is discussed in Chapter 4.

Glass carrier

White float glass from Praezisions Glas and Optik [41] is a well-suited carrier material in combination with the PI2611. It has a CTE close to that of the selected spin-on PI (PI2611). This prevents the PI from curling after releasing it from the carrier. A CTE mismatch can introduce a lot of stress in the PI layer during curing, which results in curling after release from the carrier [21].

In addition to white float glass which is used for UTCP fabrication process in the PhD work, Borofloat glass (from Schott Jena Glas [42]) is used for further research on UTCP release process. The property of the glass which is well-suited for the developement of the new release technology has been described in Chapter 6.

Adhesion promoter

The polyimide (PI2611) has a very bad adhesion on glass substrates and silicon chips. For the complete fabrication process, a good adhesion of base PI layer on the glass carrier and covering PI layer on the silicon chip is necessary. To solve this issue, an adhesion promoter (VM652) from HD Microsystems [43] is applied on the edges of

the glass carrier before spinning the PI layer. After curing of this PI, the PI film has a marginal adhesion in the middle of the substrate and a very good adhesion at the edges of the carrier. Same material is applied on the chip surface before spinning the top PI layer.

BCB as adhesive for chip placement

BCB of the Cyclotene 3000 Series from Dow Chemical [44] was selected as an adhesive material. The detailed property of this material which favours the chip bonding process is discussed in chapter 4.

2.3.2 Pyralux LF 100 as adhesive material:

For the package-to-package bonding during lamination process, the Pyralux LF 100 sheet is used which is one of the Pyralux product series [45] from DuPont Electronic Materials. This sheet is a proprietary B-staged modified acrylic adhesive and it is used primarily to bond flexible inner layers in multilayer lamination. This bondply material is not only best suited for the stacking applications due to its excellent material properties (see Table 2.1), but also recommended by ACB, a Belgian flex manufacturer [46] (one of the project partners of European SHIFT project [47]).

Table 2.1: Sheet Adhesive property versus IPC specifications for the cured film

Properties	Unit	IPC specification
Peel Strength	kg/cm	1.3
Solder resistance ($10sec$ at $288°C$)		Pass
Dielectric Constant, max. (at $1MHz$)		4
Dissipation Factor, max. (at $1MHz$)		0.05
Dielectric Strength, max. (at $1MHz$)	kV/mm	40
Insulation Resistance	$M\Omega$	10^4
Volume Resistivity	$M\Omega - cm$	10^6
Surface Resistivity	$M\Omega - cm$	10^6

As per the data sheet [45], the specified laminating conditions are given below in Table 2.2. However the exact lamination profile is set by optimizing the adhesive flow test and peeling strength test for UTCP stacking application.

These acrylic adhesives are semi-transparent in color and are coated on release paper. They retain their original properties for a minimum of one year when stored in the original packaging at temperatures of 4–29$°C$ and below 70% humidity. These materials do not need refrigeration and should be kept in clean and well protected area. Sheet adhesive changes to yellowish in color if storage conditions have deviated

from these limits. In that condition, the material has to go through practical test run before being used in production run.

Table 2.2: Lamination condition for Pyralux bondply

Curing condition	Unit
Temperature	182 – 199 $°C$
Pressure	14 – 28 kg/cm^2
Time	1 – 2 h

2.3.3 Upisel foil as top layer

For the top side covering of the stack during lamination of packages, UPISEL-N (SE1410) is used which is a non-adhesive type copper clad based on UPILEX-VT (polyimide) [48]. This is a single sided flex material with $9\mu m$ thick Copper and $25\mu m$ thick polyimide, having excellent dimensional stability and heat resistance. The UPILEX-VT (polyimide) performs high bonding ability without any use of adhesive by simple heat lamination. It has excellent peeling strength, heat soldering resistance and chemical resistance.

2.3.4 Circuit foil TW-YE as bottom layer

The bottom side of the stack has to be complete conductive layer for the through hole plating process. As the backside of the packages is only polyimide layer (non-conductive), it is not recommended to start the Copper plating process directing on this surface. A $9\mu m$ thick Copper flex (TW-YE, from Circuit foil [49]) is laminated as the bottom layer in the stacked packages. This product is a matte side treated electro-deposited copper foil, characterized by enhanced high temperature elongation properties (IPC-grade 3) and thermally stable micro-structure. Its excellent adhesion to a broad range of substrates allows it to be used for the fabrication of multi-layer lamination application.

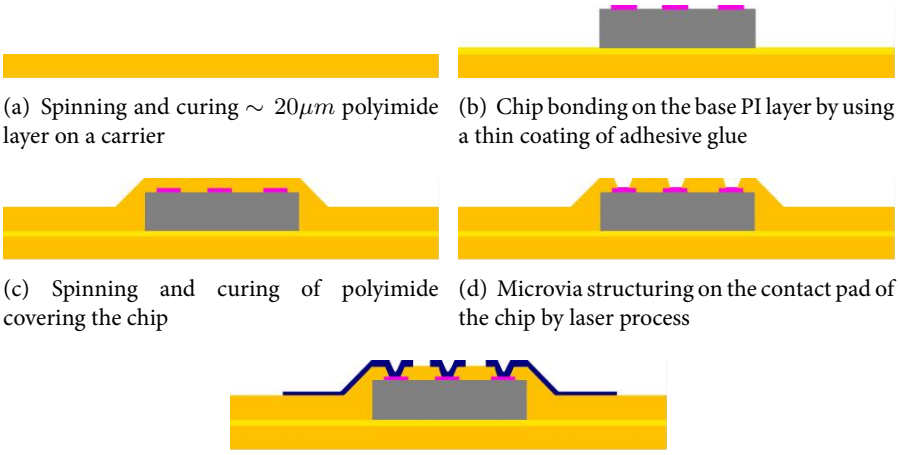
2.4 Process Development

The spin-on polyimide based UTCP technology which is the base technology for developing the whole stacking technology, was developed during the PhD work of Wim Christiaens [21]. During the European TIPS project, this technology was transferred to our Swiss based project partner HighTec MC AG [34] for industrial level production of these UTCPs to fabricate demonstrator. As per the facilities available there, the company was able to provide UTCPs with different layout structuring for the stacking process development.

The basics of this conventional UTCP technology is discussed in section 2.4.1. The further development in this technology for improving yield figure is described in Chapter 4. The basic processes in developing the stacking technology are vacuum lamination, THV formation by laser drilling, THV plating and patterning. These technologies have been optimized during this PhD work.

2.4.1 Conventional UTCP Technology

This section presents a non-photodefinable polyimide (PI) based embedding technology for 3D integration of very thin chips. The silicon chips are thinned down to $\sim$ $30\mu m$ and embedded in between two spin-on polyimide layers, resulting in a total thickness of only $\sim$ $60\mu m$. The via on the polyimide film covering contact pads of the chip are made by (Nd-YAG) laser drilling. The whole package is then metalized by TiW ($50nm$) + Cu ($1\mu m$) sputtering and Cu thickening upto $\sim$ $5\mu m$ by galvanic deposition. Metal patterning for fan-out routing on the chip is made by lithography and wet chemical etching process. The schematic process flow for fabricating these UTCPs is given in Figure 2.4. The chip, PI and metal layers are so thin that the whole package is bendable (Figure 2.5). The process development was described in details by [21].



(a) Spinning and curing $\sim$ $20\mu m$ polyimide layer on a carrier

(b) Chip bonding on the base PI layer by using a thin coating of adhesive glue

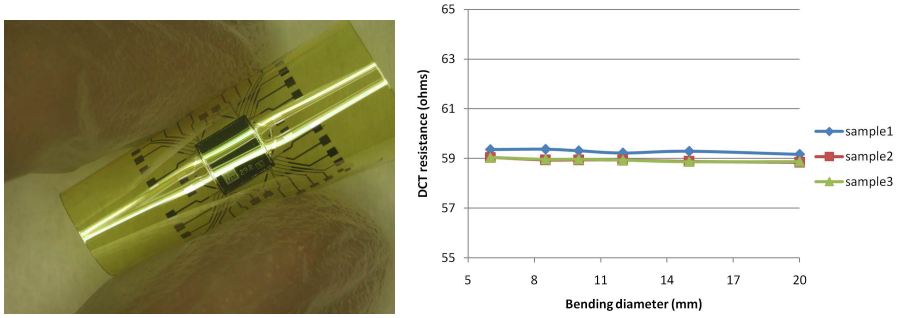
(c) Spinning and curing of polyimide covering the chip

(d) Microvia structuring on the contact pad of the chip by laser process

(e) Metallization and pattern definition on the metal surface

Figure 2.4: Process flow for producing single ultra-thin chip package in a conventional way

The UTCP bendability behavior is elaborated by [19] using photodefinable polyimide based conventional UTCP. A linear characteristics of daisy-chain resistance vs bending diameter has been achieved for the package containing PTCE test die of size $5 \times 5mm^2$ and thickness $20\mu m$. Figure 2.5-b illustrates the quantitative value of bendability where the bending diameter ranges from $20mm$ to $6mm$.



(a) Bendability of the UTCP [21]

(b) Daisy-chain (DCT) resistance as a function of bending diameter

Figure 2.5: (a) Bendability of the UTCP [21], (b) Quantitative figure for UTCP bendability [19]

2.4.2 Vacuum lamination technology

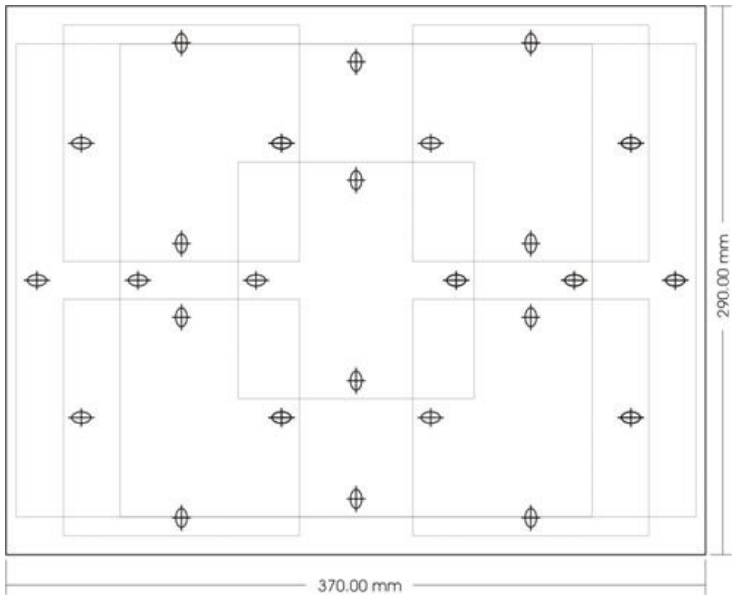
Next stage is to make a stack using the vacuum lamination process. Evaluation of this process in stacking different flex layer is described in this section. The basic set of parameters for optimizing the whole process are temperature, pressure cycle with respect to lamination time for uniform adhesive melt, flow and full cure. This is an requirement for stable bonding with minimum thickness offset within the laminated layers.

The lamination tooling system (Figure 2.6-b) in our CMST group can be used for samples of size ranging from $10 \times 10cm^2$ to $24 \times 36cm^2$ (Figure 2.6-a). There are pin holes with mechanical pins to hold the layers during lamination process, preventing misalignment within the stacked layers. Before the lamination, pin hole should be made on the substrates e.g, by laser cutting process.

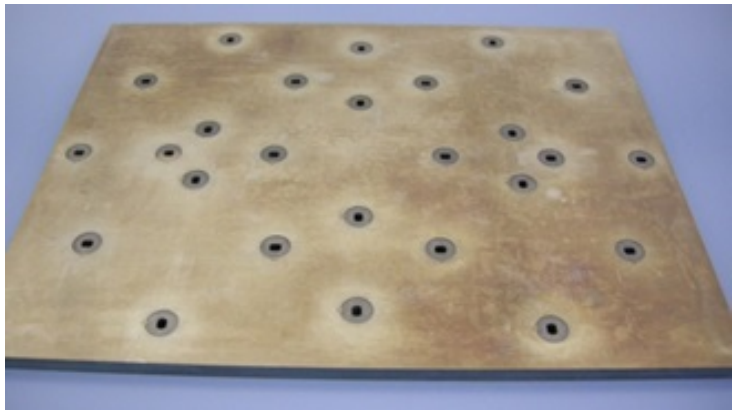
Lamination Process

According to the demonstrator's specification (which is stack of four EEPROM UTCP's), the stack is expected to include 4 separate UTCP layers with $25\mu m$ thick bonding material in between them. Pyralux LF 100 adhesive sheets are used as adhesive layers between UTCPs in the stack of having the above said thickness. The lamination process is done using the vacuum laminator (Figure 2.7).

The lamination cycle is divided into 4 regions: adhesive melt, adhesive flow, adhesive cure, and cooling down. In beginning of the cycle, a vacuum is drawn and held without pressure for approximately $15min$ until it reaches $2mbar$. During this time all the air, moisture, and other volatiles are pulled out of the pressed stack. At the completion of this pre-vacuum process, the melt portion of the lamination cycle starts.



(a)



(b)

Figure 2.6: Layout of a tooling plate with registration holes

At the beginning of the *melt* (at $90°C$), the adhesive is solid and pressure should be low. This low pressure is known as *kiss pressure*. In the current process, kiss pressure is selected as $50N/cm^2$ and this continues for approximately $15 - 20min$. Heating rate of the cycle is $5°C/min$. The *flow* portion of the cycle begins when adhesive liquefies at $130°C$, before its viscosity begins to rise due to curing. At the beginning of the flow, full pressure is given as $25kg/cm^2$. After the flow stage, adhesive *cure* is proceeding. Temperature is held at its maximum value ($195°C$) or curing temperature and it

continues for $90min$. Last part of the cycle is the cool down cycle. The lamination profile with graphical illustration is given in Figure 2.8.

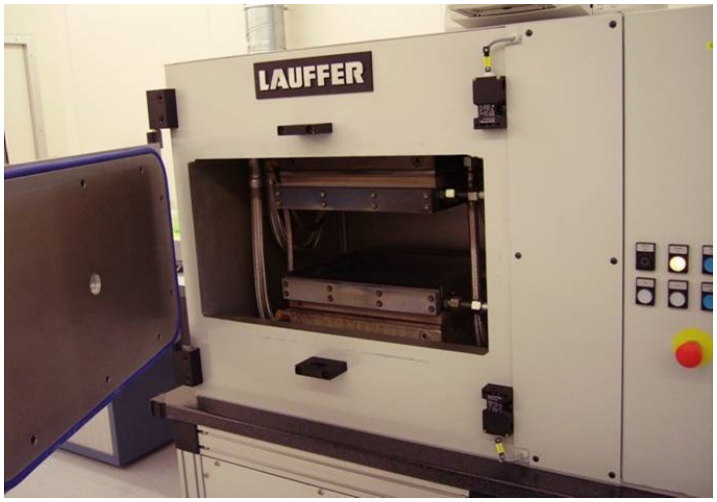


Figure 2.7: Lauffer (type RLKV 25) vacuum laminator as installed in our cleanroom

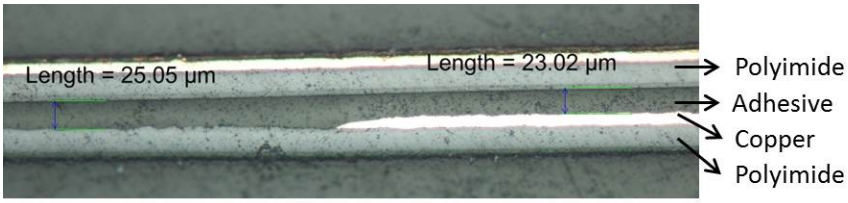
Figure 2.8: Temperature and pressure cycle during the vacuum lamination process

To evaluate this lamination process using Pyralux LF 100 as adhesive material, following tests were performed.

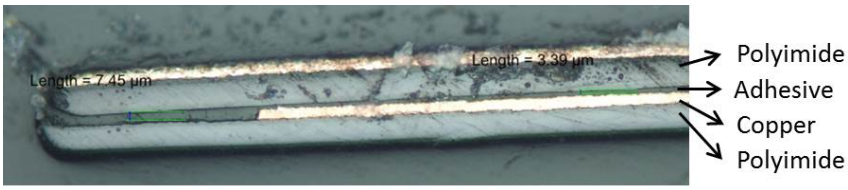
Adhesive flow test

To study the adhesive thickness uniformity within the stack of polyimide and patterned copper some experiments were executed by using commercially available Upisel-N foils (SE1410) as dummy package. All the layers to be laminated were cut into sizes of $10 \times 10cm^2$ before starting the processing. One of the single sided foils is patterned on the copper side by $3mm$ strips facing the adhesive sheet and used as bottom layer of the stack (as described in the Figure 2.9). Top layer foil was placed over it with polyimide side facing the adhesive material.

Figure 2.9: Schematic cross-section of different layers used for adhesive flow test



(a) The central part of the stack showing uniform spread of adhesive of thickness ranging from $25\mu m$ to $23\mu m$

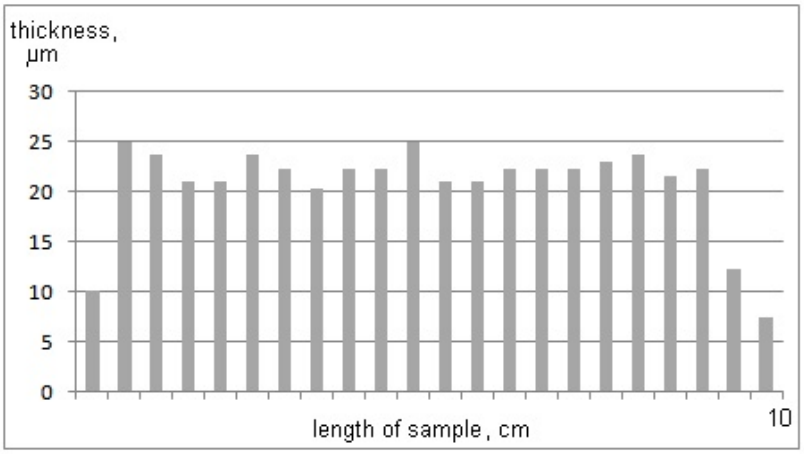


(b) Edge of the stack showing adhesive squeezing out leaving minimum thickness of around $5\mu m$

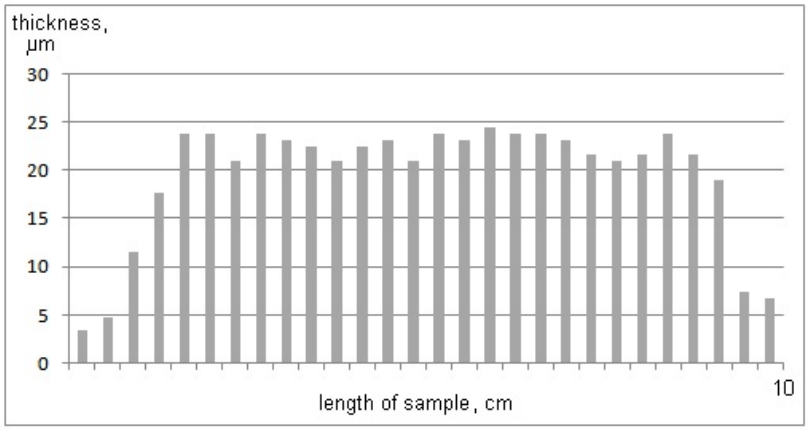
Figure 2.10: Adhesive layer thickness uniformity within the stack

The lamination parameters for the adhesive curing process for this experiment was maintained at $195°C$ temperature, $26kg/cm^2$ pressure for $2h$. From stack

cross-section view in Figure 2.10, the adhesive layer uniformity can be verified. At the central part of the sample, the adhesive thickness is almost uniform with a variation by a factor of $2\mu m$ at the copper pattern. The adhesive is squeezed significantly in edge area of samples. The whole picture of this thickness distribution is given the chart for the adhesive flow in the Figure 2.11.



(a) Adhesive layer thickness over the polyimide surface



(b) Adhesive layer thickness over the copper surface

Figure 2.11: Evaluation of adhesive layer thickness uniformity within the stack, made referring to the measurements shown in Figure 2.10: (a) over the polyimide surface, (b) over the copper surface

Adhesion test

The Dage Series 4000m in CMST is dedicated for peeling strips of width around $3mm$ at an angle of 90° from the underlying layer. For this test, the layer to be peeled off is patterned as strips of $3mm$ width and has to be thicker enough for clamping before peeling. One end of this strip is clamped and pulled up at a constant speed of $500\mu m/sec$. The force applied is recorded and the average force after $2mm$ peeling is used for calculation. Peel strength is expressed by dividing the minimum force with the width of the strip, so its unit is N/mm.

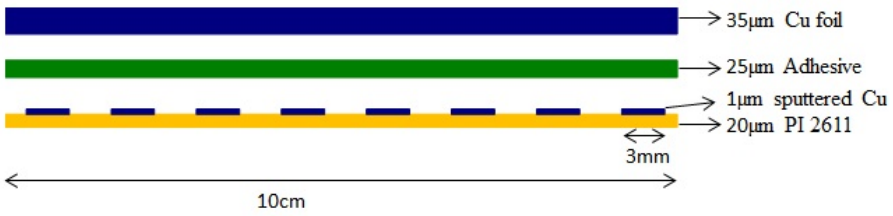


Figure 2.12: Schematic cross-section of different layers used for layer to layer adhesion test

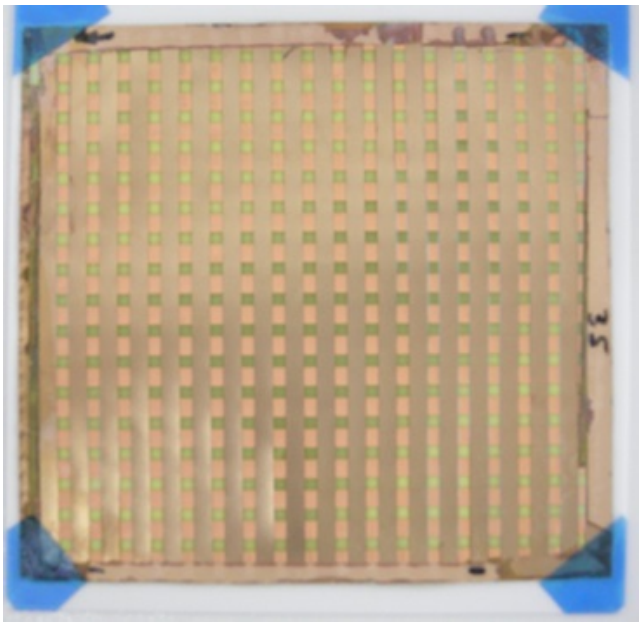
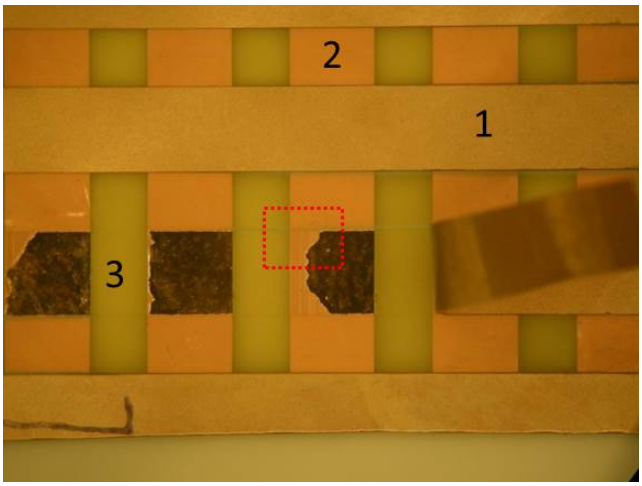
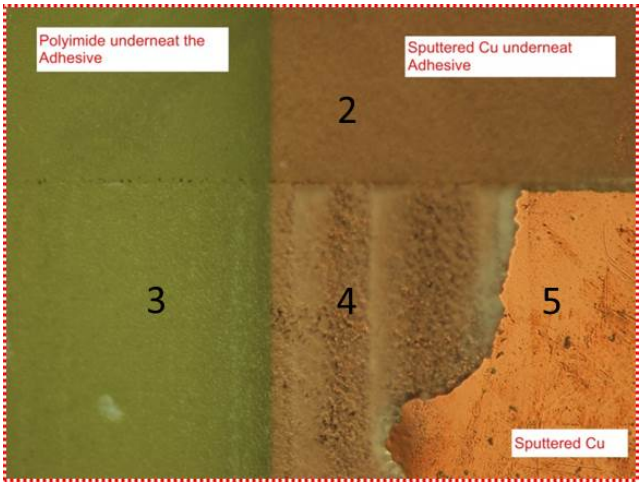


Figure 2.13: Sample for peeling test to evaluate the layer-to-layer adhesion within the stack



(a) Peel test result: optical view of the interfacial layers



(b) Close view at the adhesion failure region

Figure 2.14: Peel test result: optical view of interfacial layers, (1) Top layer Cu strip, (2 and 4) Sputtered Cu underneath the adhesive, (3) polyimide underneath the adhesive, (5) exposed copper layer indicating poor adhesion of LF100 on the sputter deposited Cu

The layer-to-layer adhesion within the stack of different materials to be used in the demonstrator was evaluated by peeling tests. The bottom flex layer was fabricated using conventional UTCP technology by spin-coating and curing PI 2611 on 4" glass carrier to produce $20\mu m$ thick polyimide layer. As this polyimide layer has a maximum thickness of $5\mu m$ per single spin-coating step, repeated spinning steps are required to get a thicker polyimide layer ($20\mu m$). A $1\mu m$ thick copper layer is

sputter deposited and patterned into strips of width $3mm$ on this polyimide layer. After release from carrier, this layer is laminated with $35\mu m$ thick copper layer (from Circuitfoil TW-YE [49]) with the same adhesive material (Pyralux LF 100). The schematic cross-section of all these layers are shown in Figure 2.12. After the lamination, the top side copper foil was patterned as $3mm$ strip lines crossing over the bottom layer sputtered-copper strips as illustrated in Figure 2.13.

By the peeling test, the measured peel strength at the adhesive interface was found to be more than $1.2N/mm$. In Figure 2.14-b (region 5), it can be seen that the adhesive layer laminated on the sputtered copper has been detached during the peeling process. This has been observed at most of the places after peeling the entire strips of copper. However, the adhesive laminated onto the polyimide surface doesnot get ruptured in this process. From this observation, following conclusions are extracted.

- A good adhesion between adhesive layer LF100 and base polyimide PI2611.
- Comparatively weak adhesion between the LF 100 adhesive and sputtered copper.

To overcome this adhesion failure issue (Pyralux LF 100 on copper), the Cu surface should to be roughened before lamination. The standard process of Cu roughening prior to lamination is H_2O_2 based wet chemical process. This process etches the Cu upto $1-2\mu m$ and results a surface roughening of $\sim 600nm$. This requires the copper to be thickened upto $6-8\mu m$ by electroplating to compensate this factor during roughening and for subsequent processing which involves TH plating.

2.4.3 THV drilling: Laser Ablation

Once the packages with metal fan-out are laminated, the through hole vias (THV) on the stacked external contact pads are drilled by laser micro-machining. Laser ablation is a clean and fast process which makes it efficient technology for the via formation on multi-layered flexes. It is a material removal process that uses localized thermal energy caused by absorption of laser light. In general, ablation occurs when the material absorbs the light energy strongly at the laser's wavelength and the absorbed energy density is beyond the material mechanical threshold [50], [51].

There are 3 types of lasers which are normally used in microelectronics packaging application: CO_2, Nd-YAG and Excimer lasers [52]. Their individual properties are the determining factors in using them for different materials with varying via geometry. As a consequence, ultraviolet-emitting lasers - excimer and Nd-YAG laser are much more suitable for getting structures with fine pitch than their infrared counterparts (CO_2 laser). The multi-frequency property of YAG laser enables emitting radiations from near IR to UV and it is faster than excimer laser, therefore it is more versatile.

The laser set-up (Figure 2.15) in our research group is used for material structuring for opto-electronics and micro-electronics applications. The more detailed configuration of this set-up with the fundamentals of laser ablation on polymer material was given by G. Van Steenberge [53]. Microvia drilling for RCC laminate based multi-layered PCBs is studied in the framework of the European Hiding Dies Project [54], [55]. In this PhD work, THV drilling on multi-layered stack was studied upto the maximum aspect ratio (depth/diameter) of $7:1$.

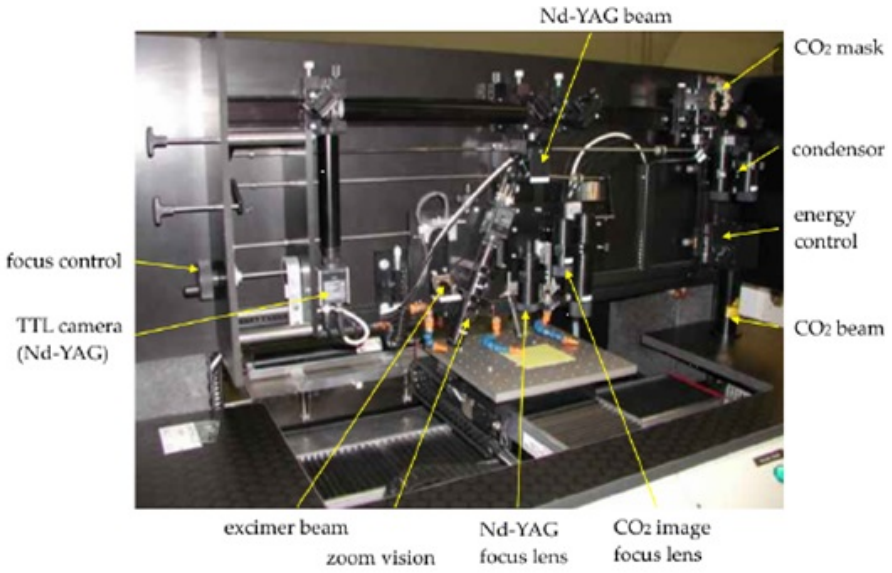


Figure 2.15: Laser set-up at CMST [53]

The Gaussian beam has the advantage of having a uniform profile which favors drilling through certain thickness of flex with minimal focal problem. Through holes of high aspect ratio are the necessary requirements for the multi-layered circuits having a very fine pitch ($< 100\mu m$). Nd-YAG laser (Gaussian beam) with trepanning drilling method is best suited for making the THVs on these stack of layers having different material threshold. In this case, the rotation of the beam spot allows making the holes of required size with nice shape. For the current approach, THVs of diameter $200\mu m$ are realized on the stack of thickness ranging from $200\mu m$ to $300\mu m$. The laser trepanning method is demonstrated schematically in Figure 2.16.

The mechanical threshold of the material is depended on the fabrication process of the stack. Therefore, it is challenging to determine the exact laser parameters for drilling through the stack containing materials of different mechanical threshold. As per the demonstrator specification, each stack should contain 4 UTCP packages. However, the exact thickness of each UTCP (conventional/ Flat) layer and the final stack build-

up were the unknown figures at the beginning of this process development. To gain knowledge on all these aspects, following experiments were performed for drilling through holes with nicely shaped THV walls.

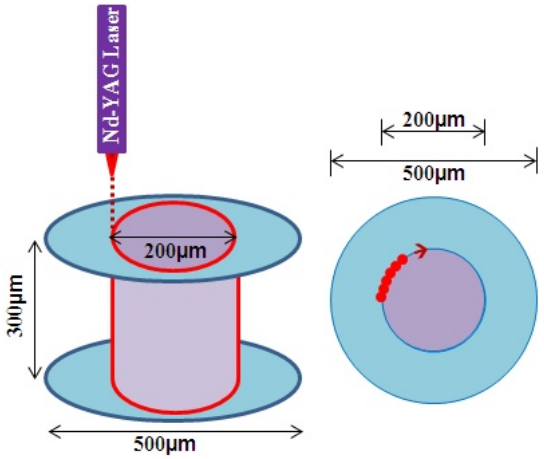


Figure 2.16: Through hole drilling process by laser trepanning method: Side view (left), top view (right)

The basic materials within this stack are given below. As the exact thickness of the stack was unknown, the initial set of layers were chosen to make of stack of total thickness $200\mu m$.

- Cured polyimide films (PI2611, HD4110, Upilex-S polyimide film)
- Copper (sputter deposited, electroplated, Upisel-N flexible copper clad [48], treated copper foil [49])
- Acrylic based adhesive material (Pyralux LF 100 [45])

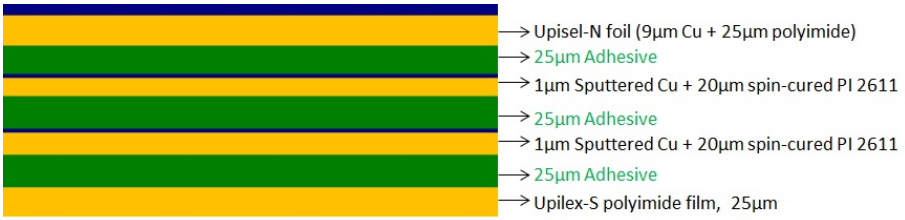


Figure 2.17: Schematic of different layers laminated for THV drilling experiments

At the beginning of this process development, the laser parameter was optimized using the stack of Upiles-N foil ($25\mu m$ PI + $9\mu m$ Cu), $20\mu m$ thick PI 2611 with $1\mu m$

sputtered Copper, pyralux LF 100 ($25\mu m$) and $25\mu m$ thick Upilex-S Polyimide film in making THV of aspect ratio $1:1$. A schematic example of different layers used for 1st set of optimization experiments is given in Figure 2.17. As per the preliminary test results, some issues such as undercutting of THs at adhesive layers, melting and sticking out of adhesive layer were observed (Figure 2.18).

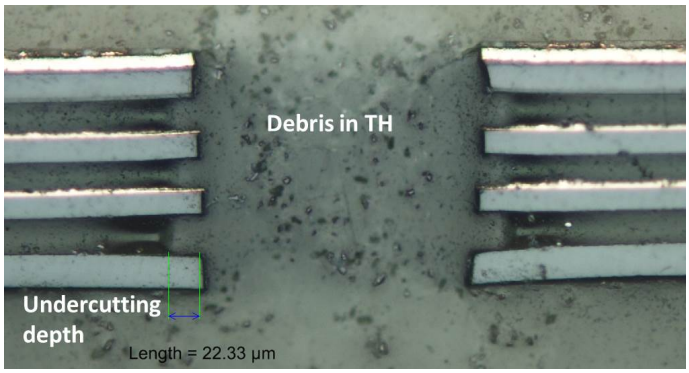


Figure 2.18: Cross-section of THV showing undercutting and smearing of adhesive

Laser parameter optimization

Important parameters for trepanning are 'pulses at a place per round', 'total pulses at a place' and 'round per sec'. Those represent the repetition rate of the laser shots. After some preliminary tests, laser power is chosen to be fixed at $500mW$ and pulse repetition rate of YAG laser at $10kHz$. Fixing those values, there are still a number of parameters which has an influence in the whole drilling process are given below.

- Laser Power (E) = $500mW$
- Pulse repetition rate (f) = $10kHz$
- Spot size of YAG laser (d) = $25\mu m$
- Pulses at a place= (n_1)
- Number of places per round (n_2) = $3.14 \times D/d$ (here D = Through Hole diameter)
- Pulses per round (n_3) = $n_1 \times n_2$
- Total pulses at a place (n_4)
- Total round (n_5) = n_4/n_1
- Total pulses to drill one THV (N) = $n_3 \times n_5$
- Round per sec (R) = f/n_3 (input parameters for trepanning)

The Gaussian beam profile of the YAG laser has been calibrated at CMST giving pulses of shot size $25\mu m$. As the beam shaping optics in our set-up is unstable, the pulse size changes within the range of $20\mu m$ to $30\mu m$ which makes it difficult to get the exact

set of parameter for laser drilling. A similar situation has been encountered with the trepanning system.

Influence of "Pulses at a place"

An experiment is set to study the influence of "pulses at a place" (n_1), in making a through hole of diameter $\sim 200\mu m$ on a stack of thickness $\sim 170\mu m$. The total pulses at a place (n_4) is dependent on the stack thickness. Higher is the stack thickness higher will be the value of n_4. The materials within the stack have a different threshold value. Therefore, choosing the right n_4 value and redistributing into total number of round (n_4) to see the influence of pulses at a place (n_1) is quit a time consuming task. The set of parameters used for this test is tabulated below (Table 2.3) with their influence on the drilling process. For this test, total pulses (N) was fixed at a value of 3000. Assuming the spot size $25\mu m$, the number of places per round (n_2) is calculated as 25.

Table 2.3: Laser parameters to study the influence of "pulses at a place"

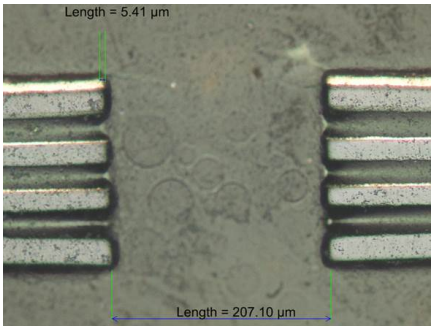
No.	n_1	n_3	n_5	R	remark
a	16	400	8	25	undercutting (max)
b	8	200	15	50	adhesive sticking out (min) and undercutting (min)
c	4	100	30	100	adhesive sticking out (moderate)
d	2	50	60	200	adhesive sticking out (max)

The result of this test put together in the Figure 2.19. The conclusion made by the cross-section analysis of the through holes are cited briefly in Table 2.3. With the fixed value of total pulses (N) and pulse repetition rate (f), the RPS value (R) is inversely proportional to the pulses at a place (n_1). Less the n_1 value, more is the rotation speed which means less the waiting time between two cycles of repeated pulses at the same place. Probably the waiting time is not enough to solidify the acrylic layer after each round of exposure which leaves smearing of acrylic material out of the THV. With higher n_1 value, the same place gets many pulses at once which probably causes excess heating at the inner layers good enough for the undercutting.

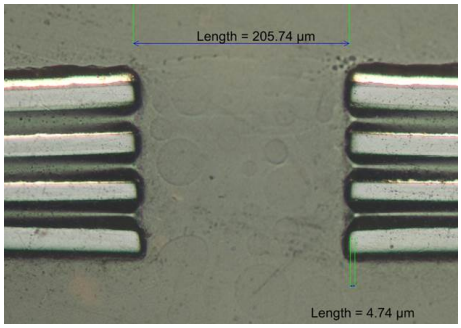
THV with higher aspect ratio

High aspect ratio of this vertical circuit is a KPI (Key Performance Indicator) of this new generation fine pitch 3D-interconnect technology. The capability of producing the through holes with higher aspect ratio has been evaluated in these multi-layered stacks. The similar experiment (as the previous one) was repeated in drilling holes on the stack of higher thicknesses $190\mu m$, $250\mu m$, $350\mu m$. Each of these stacks containing 2, 3 and 4 layers of spin-cured Photodefinable Polyimide layer (HD4110 [40]) each of

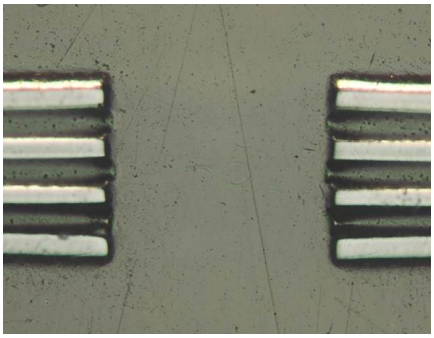
thickness varying from $30\mu m$ to $50\mu m$ with $10\mu m$ thick copper (sputtered + galvanic deposition).



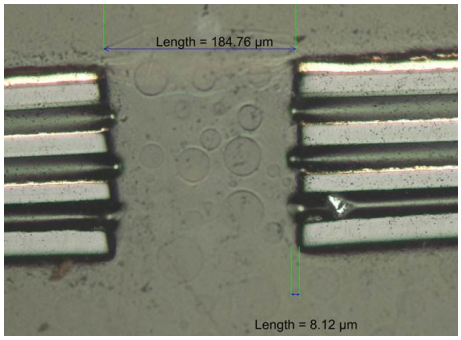
(a) maximum undercutting



(b) minimum undercutting and adhesive sticking out



(c) moderate adhesive sticking out



(d) maximum adhesive sticking out

Figure 2.19: Cross-section of THV showing influence of "pulse at a place" (n_1) with fixed total pulses (ref: Table 2.3)

At the beginning of these experiments, the THV diameter was fixed at $200\mu m$ to verify the effect of laser parameters (power and total pulses at a place) on the 1st stack of thickness $190\mu m$. As per this test, the holes were found not completely through the stack for low power ($300mW$) and completely through for higher laser power ($500mW$). By increasing the total pulses (n_4) at a place, due to excessive heating deformation level in the top side copper surface increases and that does not have any influence by changing the pulses at place (n_1). The final set of parameters for drilling holes of diameter $\sim$ $200\mu m$ in a stack of thickness $\sim$ $190\mu m$ are given in Table 2.4. The power and pulse repetition rate were set at $500mW$ and $10kHz$, respectively.

The same set of parameters was implemented in drilling holes of different diameter on a stack of thickness $350\mu m$. The objective of this experiment was to evaluate the whole

drilling and plating process in making TH interconnection of aspect ratio ranging from $7:4$ to $7:1$. The diameter of the THVs was varied from $50\mu m$ to $200\mu m$ with an increment of $25\mu m$. As the stack thickness was the same for all the tests, the total pulses at a place (n_4) was fixed at 400. Looking at the previous results, pulses at a place (n_1) was fixed at 10. This means total number of rounds (n_5) made by trepanning process were 40. As per the previous assumptions, power and pulse repetition rate were set at $500mW$ and $10kHz$, respectively.

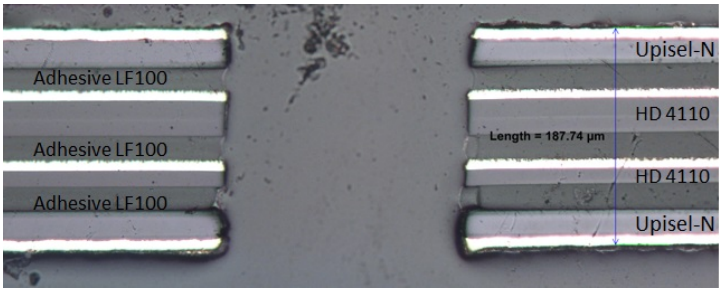


Figure 2.20: Cross-section of THV drilled with optimized set of parameters

Table 2.4: The optimized set of laser parameters for making THV of diameter $200\mu m$ shown in Figure 2.20

Pulses at a place	Pulses per round	Total rounds	Total pulses at a place	Total Pulses	RPS
10	250	20	200	5024	40

During these tests, a mild fluctuation in the trepanning rotation accuracy has been noticed which at the end gives rise to a via of dimension differing slightly of the desired size. The THV dimension from top and bottom side of the stack were measured by optical microscope.

Another thing which has been noticed is that thicker the copper on the UTCP, less is the undercutting depth of adhesive film. The copper layer in between the acrylic layer and polyimide layer thus acts as heat spreading layer during this laser ablation process and prevents excessive melting of adhesive film. This has to taken into account in the design phase of the UTCP which has to be 3D-stacked afterwards. And this effect becomes more severe when no copper layer is used on the polyimide film.

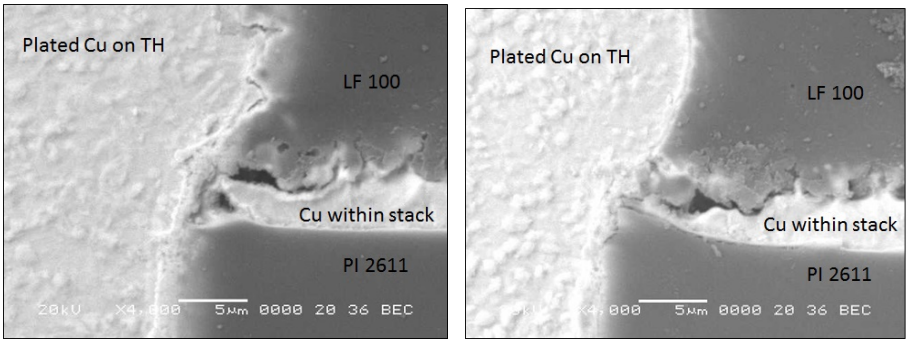
2.4.4 THV plating

The next step after the drilling process is the through hole plating process. This plating process is a wet chemical process which consists of a cleaning and a Cu micro-etching

step, followed by initial metallization of the surface and through holes by electroless copper deposition and a subsequent electrolytic copper plating step. But the wet cleaning process is not sufficient enough for the removal of organic debris on the THV wall created by melting of the acrylic layers due to the thermal effect. This has been verified by cross-sectional analysis of some plated through holes.

Desmear Process

Plasma etching is the quickest, cleanest and most reliable way to desmear acrylic adhesive based TH's in the flex. The etching of debris was done using Plasma Therm Batchtop RIE machine which can dry etch thin layers at room temperature. As reported by DuPont electronics [56], a first step with a CHF_3/O_2 gas mixture in an RIE chamber performs the etching of debris and the second step is a pure oxygen burn process in which the fluorine bound organics on the hole wall get removed. But there are quite a lot of other parameters which has an influence on adhesive etch back, e.g., RF power, chamber Pressure, Gas mixture composition, Gas flow rate (sccm).



(a) Cu plating on rough adhesive wall (b) Cu plating on smooth adhesive wall

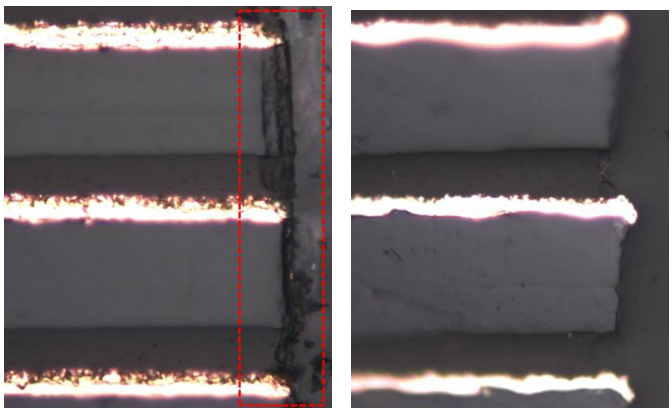
Figure 2.21: SEM analysis of plated though hole at the Cu-interconnect (desmeared with RF power 200W): void trap in both the cases

A number of experiments were performed to investigate the effect of these parameters in the desmearing process. 1st experiment was to check the influence of RF power (by varying it from $100W$, $150W$, $200W$) with fixed chamber pressure ($100mTorr$) in oxygen plasma with O_2 flow rate of $25sccm$ for $10min$. As the THVs are of aspect ratio $1:1$ or higher, the through hole samples were exposed to the RIE both from top side and bottom side with the same set of parameters. The samples were evaluated after the full plating process. By analyzing the whole process, following conclusions were drawn.

High power ($200W$) during RIE process gives best result in desmearing process, but at some point a loss of contact has been noticed as shown in the Figure 2.21. The probable reason could be O_2 plasma which was used for longer duration ($10min$ for top side + $10min$ for bottom side). The Cu within the stack exposed to this RIE

process can get oxidize and can be etched in a faster rate than usual rate during the wet etching process. As wet chemical based micro-etching is a necessary step before the Cu-plating, the fast etching of this oxidized Cu cannot be avoided. In addition to that, some chemical agents in electroless plating process blocks the space at the interconnection region which can be identified from the dark mark in the SEM analysis pictures (Figure 2.21).

The stack contains several layers of polyimide, acrylic compound based adhesive layers and copper. It is quite challenging to choose which combination of gas mixture can clean the THV perfectly without affecting the individual layers within the stack. As mixtures of $CHF_3(20\%)$ + $O_2(80\%)$ are known to be used in RIE for polyimide surface roughening, this combination are supposed to clean the THV walls. Keeping the power $(150W)$ and pressure $(100mTorr)$ fixed, time was varied and also double step process was introduced this time to see the effect.



(a) (b)

Figure 2.22: Cross-section of desmeared THV (a) by single step process in presence of gas mixture CHF_3 $(5sccm)$ + O_2 $(20sccm)$ for $2min$ (b) by double step process in presence of gas mixture CHF_3 $(5sccm)$ + O_2 $(20sccm)$ for $2min$ and only O_2 $(25sccm)$ for $1min$

Some dirt particles on the THV walls were found on the samples processed with single step RIE cleaning. Undercutting in the adhesive layer and roughening in the PI layer were higher for higher processing time. A huge difference in THV wall surface was observed by adding $1min$ O_2 plasma treatment (double step process). The result of this experiment concludes that the gas mixture used for $2min$ is enough for roughening the THV wall without making any damage to different layers (Figure 2.22-a). Also $1min$ O_2 plasma treatment afterwards ensures the complete cleaning of the THs (Figure 2.22-b). As the O_2 plasma during RIE has some bad effect on the Cu (which is not known quantitatively), the etching time should be as minimum as possible if we

consider single step process with the condition that time must be enough for complete cleaning of the THV.

Copper Plating Process

Electroless copper plating is performed first to provide a thin conductive layer on the hole wall. Good plating results have been obtained with the following Shipley process parameters (Table 2.5).

Table 2.5: Electroless Cu plating parameters

Steps	Chemical Agent	Process Parameters
Conditioning	Conditioner 3323A	$5min$ at $45°C$
		Double rinse in DI water ($2min$)
Cu μ-etching	Circuposit 3330	$1min$ at RT
		Double rinse in DI water ($2min$)
		with and without USA
		Changing sample holder
Precatalyzing	Pre-dip 3340	$1min$ at RT
		No rinse in DI water ($2min$)
Catalyzing	Catalyst 3344	$4min$ at $35°C$
		$2min$ rinse in DI water
		Changing sample holder
Electroless	3350-1	$45min$ at $47°C$
Cu plating		$2min$ rinse in DI water at $35°C$
Antitarnish	Cuprotec 3	$3min$ at RT
		Double rinse in DI water ($2min$)
Annealing		$30min$ at $120°C$

The electroless Cu bath has a very limited life-time. Without replenishing the bath, the compounds go out of working-range. After evaluating the whole chemistry behind this process, it was recommended to replenish the bath with an interval of $45min$. For the specific process (THV plating), the sample is set to swing in the central part of the plating bath which allows the chemical reagents to flow through the higher aspect ratio vias and enhances the plating on the non-conductive walls activated by catalytic process. With this set of parameters, a Cu seed layer of thickness $\sim$ $3\mu m$ can be deposited over the entire surface of the sample. This includes the drilled THV walls and external surfaces (top and bottom side of the stack). To thicken the Cu by this process is time consuming as the plating rate is very low ($\sim 4\mu m/hour$).

Table 2.6: Galvanic Cu plating parameters

Steps	Chemical Agent	Process Parameters
Acid wash	PC Cleaner	$5min$ at RT
		Thoroughly rinsing in DI water
Cu μ-etching	Circuposit 3330	$10s$ at RT
		Rinse in DI water ($2min$)
		Changing sample holder
Acid Dip	10% H_2SO_4	$1min$ at RT
Electroplating	$CuSO_4$ solution	Dependent on sample size
		and required Cu thickness
		$2min$ rinse in DI water
		Changing sample holder
Antitarnish	Cuprotec 3	$3min$ at RT
		Double rinse in DI water ($2min$)
Annealing		$30min$ at 120°C

The electroplating bath at CMST allows to increase the thickness of the copper to a final value of 10-12 μm with the set of parameters listed in Table 2.6. For the double sided plating of copper on the stacked packages with THV, the value for the plating current and time have to be set by calculating the plating area of the sample required copper thickness, respectively. An example of nicely plated through hole is shown in Figure

2.23.

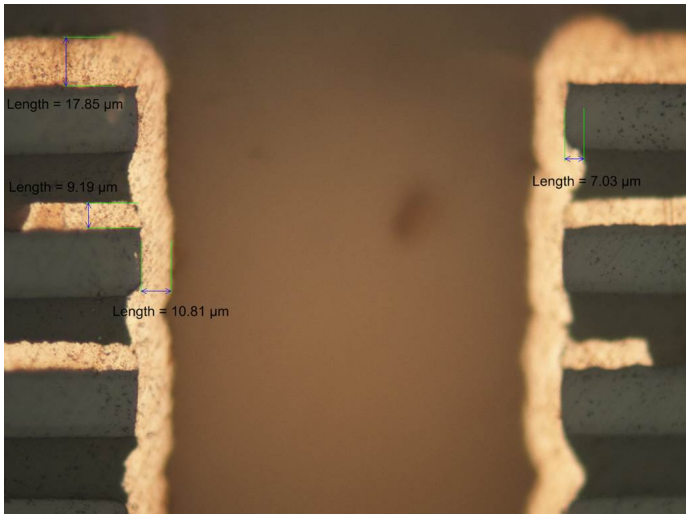


Figure 2.23: Cross-section of plated THV

2.4.5 Cu Patterning

For the Cu patterning of top and bottom side of the stack, $20\mu m$ dry film resist Riston FX920 from DuPont ™ [57] is used. Some extra THs (of size $300\mu m$ and $500\mu m$ diameter) are made on the stack as alignment marks for the final patterning. To check the resist pattern on the Cu after development, a test run was done with FR4 sheets. It was observed that with increasing UV illumination energy (from $60mJ/cm^2$ to $63mJ/cm^2$) the size of the pattern on Cu is increasing which is one of the properties of negative resist. As the Cu thickness is considerably high ($\sim$ $25\mu m$ on top and bottom), the risk of under-etching is also higher. So, the illumination energy was set at $63mJ/cm^2$ for getting a bit oversized pattern on the copper to restore the final dimension after etching.

2.5 Conclusion

The process development for stacking of conventional ultra-thin chip packages by using vacuum lamination and through hole interconnection technologies is discussed in this chapter. There is still lot of room for improving and optimizing certain steps and the set of parameters for better result, such as laser ablation process for making THV having a higher aspect ratio. With these developed process step and stacking concept, first demonstrator was realized which is a stack of 4 EEPROM memory die packages. The fabrication process and related issues are discussed in chapter 3.

Chapter 3

Stacking of Conventional UTCPs

3.1 Introduction

This chapter describes the preliminary approach in producing demonstrator which is stack of four EEPROM die UTCPs. The fabrication process includes UTCP [18], [19], [58], package-on-package (PoP) [15], [59] and through hole via (THV) [29], [30] technologies. As discussed in chapter 2, UTCP technology has the capability to produce thin flexible chip package of thickness upto several tens of micron. The use of the PoP concept enables stacking of four sheets of such chip packages by vacuum lamination. This process is similar to the Printed Circuit Board (PCB) manufacturing process, which is a cheap and fast way of producing such stacks. Package to package interconnections are made by drilling THVs by laser ablation in the outer contact pads of the stacked packages, followed by metallization of these THVs by Cu electroless deposition and electroplating. Top and bottom side Cu patterning followed by dicing produces individual chip stacks with a total thickness of $300\mu m$, embedding 4 thin dies within it.

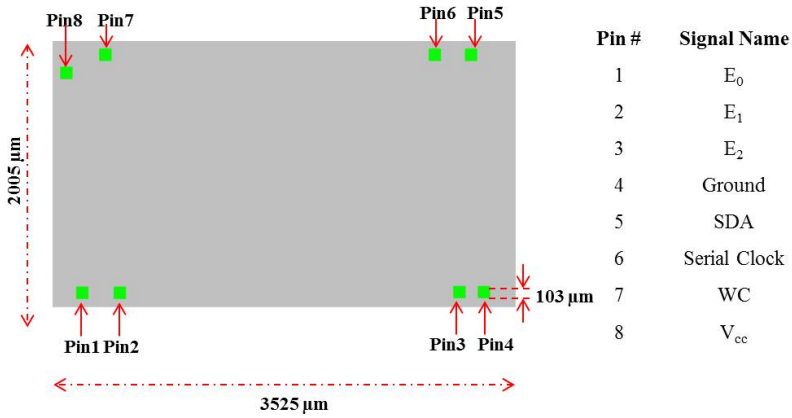
As discussed in chapter 2, each and every process has its own benefits and drawbacks. By careful selection of the materials with their respective properties, the first demonstrator was fabricated with the developed technology based on PI 2611. The most critical factors during stack production stage was through hole drilling process. Use of 2-Polyimide layed conventional UTCP for stacking leads to huge loss in stacking yield. This is going to be discussed in the failure analysis section and scope of further development in this technology for future application will be explained in great details.

3.2 3D-Stack Design

The stack layout structure was designed following the basic PCB design rules. The 2D-circuit containing four IC is redistributed in making 3D-stack design.

3.2.1 Chip Layout

EEPROM chips are commercially available memory dies used in Hearing Aid Devices manufactured by Oticon [60]. As per the coordinate specification in Figure 3.1, the die size is $2005\mu m \times 3525\mu m$ with 8 contact pads per chip having pad size $103\mu m \times 103\mu m$. The aluminium finished contact pads are bumped with $5\mu m$ thick electroless plating of Ni/Au which is a standard process offered by PacTech [61]. The subsequent thinning and dicing are handled by Disco [62] who offers a dicing-by-thinning process [37] especially suited for ultra-thin dies $(20\mu m)$.



Pin #	Signal Name
1	E_0
2	E_1
3	E_2
4	Ground
5	SDA
6	Serial Clock
7	WC
8	V_{cc}

Figure 3.1: EEPROM chip layout with contact pad specification, which are used as a reference during the process of 3D-stack layout designing

3.2.2 Package Design

The I/O limits of the package to be stacked are restricted by the following considerations:

- The pitch of the contact pads on the chip is limited by the etching technology used to pattern the copper metalization [18], [58], pitch values down to $80\mu m$ are achievable without yield loss.
- The number of I/O's is limited by the area which is taken by the fan-out, based on the sizes of the THVs, the landing pad area and track-to-track spacing.
- The parameters mentioned in the previous consideration are limited by the package to package shift during lamination process.
- Laser ablation and the subsequent plating processes limit the size of the through hole via which can be realized.

As per the 2D-circuit design, there are 8 contact pads per IC from which only 7 are used for making interconnection. The layouts for fan-out metallization in UTCPs are

adapted from this basic circuit design which contains 6 I/O's per package. Considering the above said I/O limitations for the stacking approach, the design was made for the production of multiple UTCPs (18 rows, 10 columns) on 6 " square glass substrate. Each of the single UTCP packages has 6 I/O (2 on one side, 4 on other side) of size $500\mu m$ diameter and conductive lines of width $115\mu m$. Four different lay-outs were designed (as shown in Figure 3.2) for the four different ultra-thin chip packages to be stacked after wards.

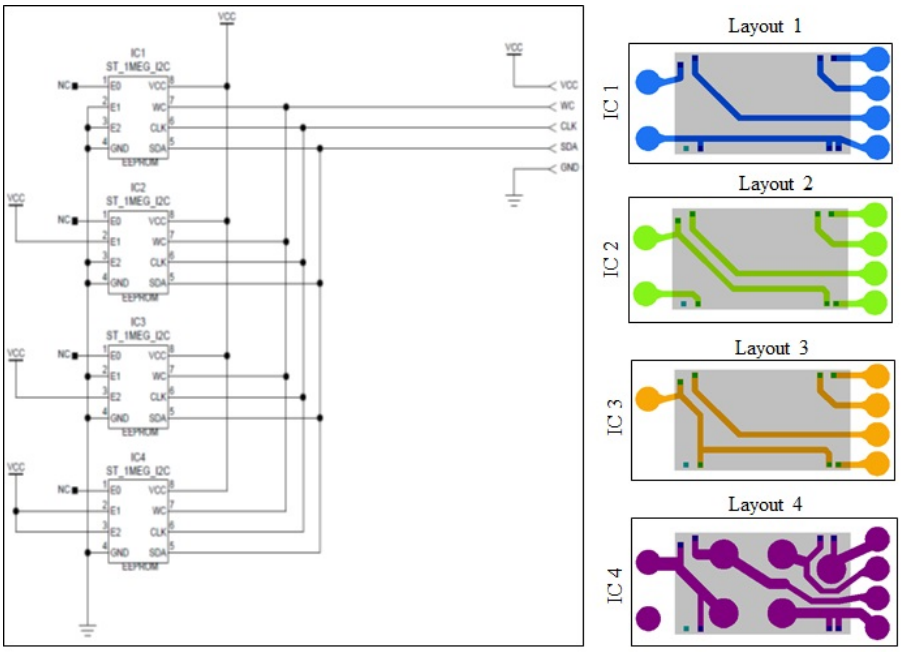
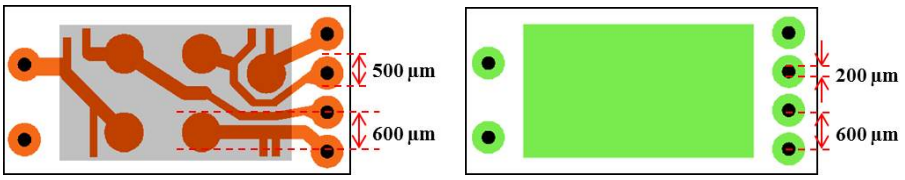


Figure 3.2: 2D-Interconnection layout for 4-EEPROM chips and the corresponding pattern adapted for making 3D-integrated stacks

3.2.3 Stack Design

As per the stacking process flow described in Figure 3.4, top and bottom layer patterning is the final processing step. The top layer used here is the exact copy of the design made for layout 4 (top most layer with contact pads for testing). The bottom layer design is made only to protect the PTH and some extra copper on the bottom side of the stack to make it more thermally stable (Figure 3.3). The top pattern contains solderable pads of size $600\mu m$ diameter for mounting it on PCB and testing purpose.



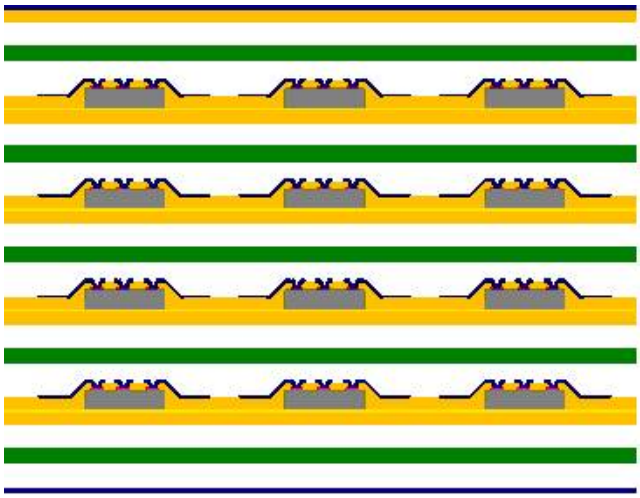
(a) Top side metal pattern (b) Bottom side metal pattern

Figure 3.3: Top and bottom side metal pattern for EEPROM stack

3.3 Fabrication Process

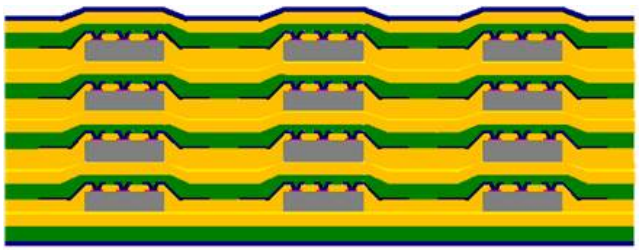
An overview of the process flow for the stacked UTCP technology is shown in Figure 3.4. The base materials for the production of stacks are UTCPs with identical or differing fan-out patterns. From cost point of view, production of multiple UTCPs on a single panel is mandatory for achieving 3D-integration of chip packages by stacking technology and precise placement of chips on a base substrate is one of the important steps which can affect the package production yield.

(a) Step 1. Production of individual sheets of Multiple UTCPs

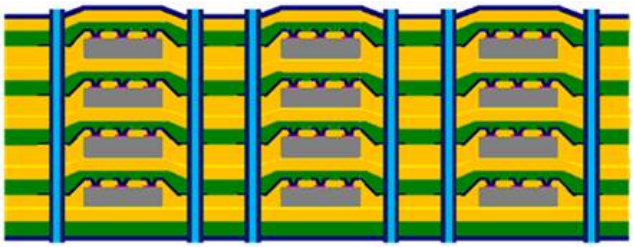


(b) Step 2. Well aligned sheets of UTCPs and extra copper flexes at top and bottom with adhesive films in between

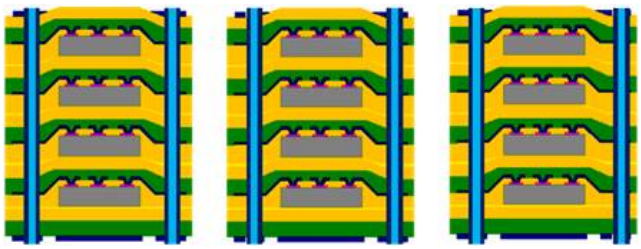
Figure 3.4: Process flow for stacking of conventional UTCPs (continued)



(a) Step 3. After stacking of all layers by vacuum lamination technology



(b) Step 4. Through hole drilling on contact pads of the embedded packages by laser ablation, followed by metallizing them by electroless/ electroplated Cu deposition



(c) Step 5. Dicing of individual stacks by laser cutting after top and bottom side metal patterning

Figure 3.4: Process flow for stacking of conventional UTCPs

After testing the yield, these packages are released from the carrier and stacked together with thin adhesive layers in-between by vacuum lamination technology. For top and bottom metallization layers, two extra Cu-flexes are laminated on both sides of the stack. Interconnection within individuals packages are made by making through holes on the outer contact pads of the stacked UTCPs, followed by an electroless/ electroplated copper deposition.

3.3.1 Multi-UTCP Fabrication

The UTCP process flow is reported by many of the researchers of our group in past couple of years [18], [19], [28], [58], [63], [64]. In the frame work of EU-funded TIPS project [65], the technology of fabricating UTCPs in industrial scale was transferred to Switzerland based project partner, HighTec MC AG [34] to supply UTCP samples for stacking experiments. As per the industrial experience, a salt based release technology for the UTCP release of carrier was adopted in this production process. Although the PI 2611 has a marginal adhesion at the glass carrier, an additional salt layer in between them facilitates the UTCP release process.

(a) Step1. Release layer deposition on the rigid carrier

(b) Step2. Spinning and curing base polyimide layer

(c) Step3. Placing chips precisely on spin-coated adhesive material and chip bonding during glue curing

(d) Step4. Spinning and curing of covering polyimide layer

(e) Step5. Micro-via opening on contact pads of chips

(f) Step6. Metallization and patterning

Figure 3.5: Process flow for conventional way of fabricating multi-UTCPs

In the conventional UTCP technology as illustrated in Figure 3.5, active components are thinned down to $\sim$ $20\mu m$ and embedded within two spin-on polyimide layers each of $\sim$ $20\mu m$ thickness. In this process, the base layer (polyimide) is spun and cured on a rigid carrier (glass). The ultra-thin dies are picked and placed on an adhesive material which is spin-coated on the cured bottom polyimide layer and cured during the chip bonding process. The adhesive material used in this process flow was the same polyimide (PI2611) as the base layer for the CTE compatibility

reason. Finally the chips are fully embedded by spinning and curing a top polyimide layer. The connection to the outer world is made by opening micro-vias on the contact pads of the embedded chips. This can realized by laser drilling, dry etching or photo lithography (when photosensitive polyimide is used). Metallization is done by sputter deposition of TiW ($50nm$) + Cu ($1\mu m$) as seed layer, followed by the electroplating of copper up to a thickness of $\sim 5\mu m$. The patterning of metal is done by a wet-etching process in combination with lithography.

The 4 panels of UTCPs fabricated by HighTec and used for the stacking process are shown in Figure 3.6. All of them are processed on glass carrier of dimension 6 " square with $500nm$ thick thermally evaporated potassium chloride (KCl salt) as release layer.

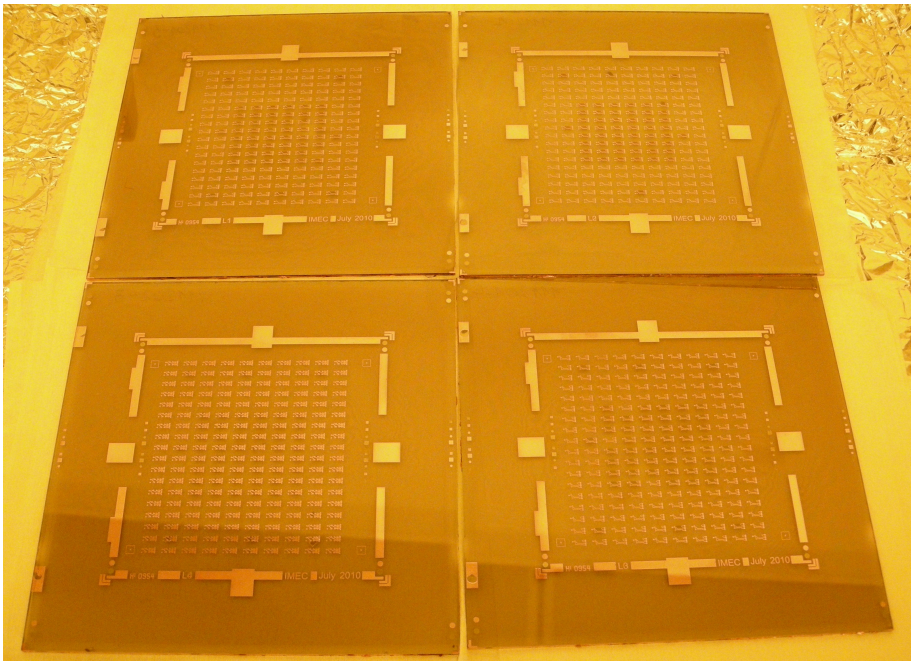
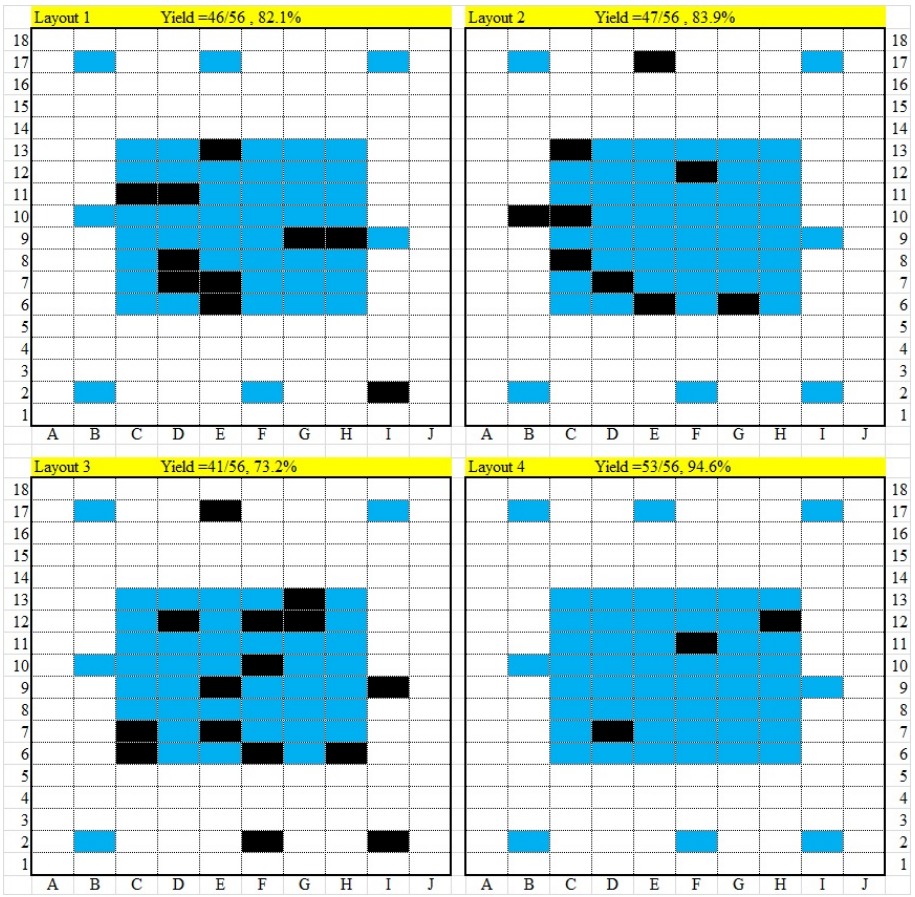
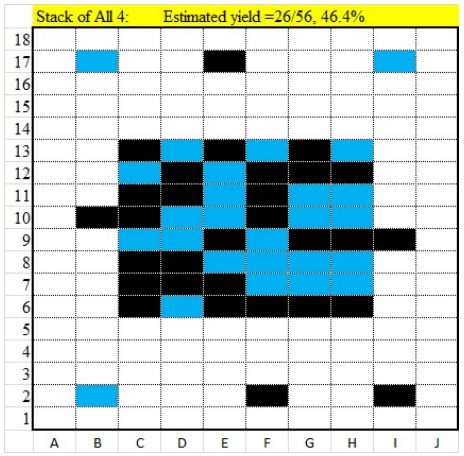


Figure 3.6: Four panels of fully processed UTCPs from HighTec company

After processing, the electrical connectivity and/or functionality of the UTCPs can be tested on the fan-out metalization, in order to create a mapping of functional chip packaged on each substrate. This process makes it easy to sort out the non-functional stacks before starting the stacking process. In the current process of fabricating EEPROM UTCPs of 4 different metal layout structures on 4 different panels, the average yield per panel was calculated to be $\sim 83.5\%$. The mapping of functional and non-functional ones are denoted by blue and black marks in the Figure3.7-a. From these values, the percentage of functional stacks is calculated as 46% and shown in the mapping Figure 3.7-b.



(a)



(b)

Figure 3.7: (a) Functional Package mapping on each panel of UTCPs, (b) Estimation of number of functional stack from the yield figure per panel

For the mechanical alignment of the package-on-package during lamination, four pin holes are made on each sheet of UTCPs by YAG laser. Additionally, laser cutting at the edges of each sheet is performed for easy release of the UTCP sheet from its glass carrier. Figure 3.8 shows the layout for this laser cutting process. The parameters used for this laser cutting process is given in Table 3.1.

Table 3.1: Laser Parameters for UTCP Release Process

Laser	Laser Power	Laser Speed	Ablated surface
$355nm$	$500mW$	$2.5mm/s$	making holes on
YAG			PI($30\mu m$)-Cu($7\mu m$) surface
		$5mm/s$	cutting PI($30\mu m$)

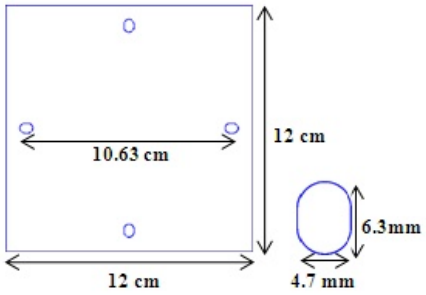


Figure 3.8: Layout for alignment holes on UTCP sheets (left), size of each hole (right)

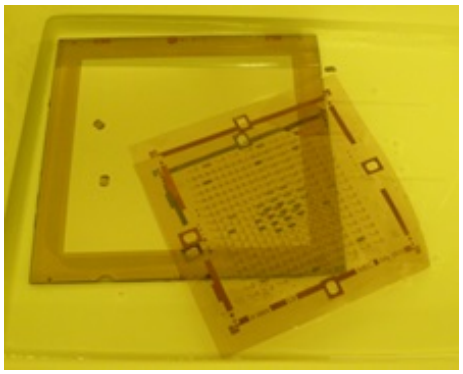


Figure 3.9: Multi-UTCP sheet release process

The release of the multi-UTCP sheets from the carrier is realized by soaking the samples in de-ionized water. The cuts made at the edges of the UTCP sheet enable water penetration under the package. Due to the hygroscopic nature of the salt situated in-between the carrier and the UTCP sheets, the water is absorbed underneath the polyimide film, and the salt gets dissolved. This effect ensures an easy release of the UTCP package sheets. This whole process is described by Wang et. al., [19]. Figure 3.9 shows the individual UTCP sheet release process by soaking it in de-ionized water.

3.3.2 Vacuum lamination process

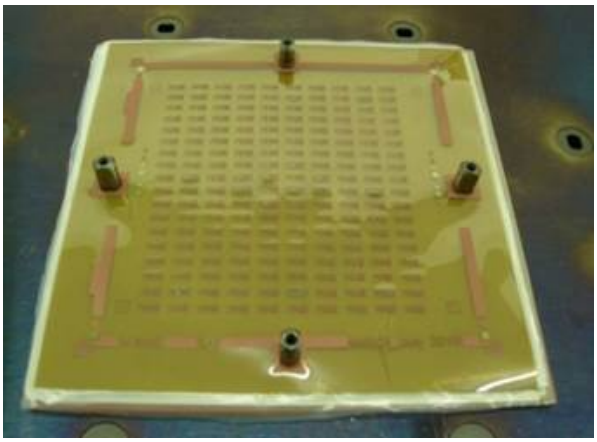
In order to improve the adhesion of the acrylic adhesive (LF 100) on the conductive copper lines on UTCPs within the stack, it is mandatory to prepare the copper surface prior to lamination. H_2O_2 based wet chemical treatment roughens the surface and also creates an oxide containing group on the copper surface which makes it beneficial for its adhesion with acrylic material during lamination process. Sheets of $25\mu m$ thick Pyralux LF100 adhesive are used in between each UTCP sheet for realizing a stable bond, as well as between the UTCP sheets and additional flex (top and bottom) layers (Step 2 of Figure 3.4).

Prior to lamination, the LF 100 is patterned according to the pattern in Figure 3.8, using laser ablation. Finally all UTCP, adhesive and metal layers are placed on a dedicated lamination plate and held in place by mechanical pin holes at the four edges to avoid shifting during the lamination process (Figure 3.10-a).

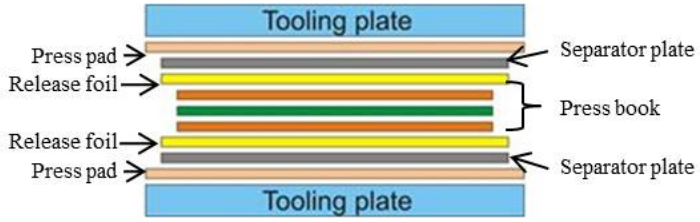
The lamination process is similar to a standard PCB lamination process. During lamination, the stack of functional layers is sandwiched between press pads, separator plates and Teflon foils, as indicated in Figure 3.10. The press pad, a soft material (Senpad), and the steel separator plates provide an even distribution of the pressure during lamination. The Teflon foil is used as a release liner to protect the laminated stack of UTCPs. The process parameters for this vacuum lamination process is indicated in section 2.4.2 of chapter 2.

A good adhesion at the interface of the LF 100 layer and polyimide (PI 2611) has been verified by peel tests. The measured peeling strength is $1.2N/mm$ or higher. The accuracy of the alignment between the different layers was verified after lamination with a layer-to-layer shift of $20\mu m$ in maximum. As the landing pads for the vias in this technology have a radius of $100\mu m$ and higher, this shift is acceptable.

The photograph in Figure 3.11 illustrates a cross-section of 4 stacked packages. It can be observed that the adhesive layer thickness is different within the chip packages ($\sim 13\mu m$, Figure 3.11-a) and on the remaining parts of the stack ($\sim 24\mu m$, Figure 3.11-b). By application of pressure during the flow process, the liquefied adhesive flows away from the chip region, where the single UTCP layers are thicker. This phenomenon reduces the overall thickness variation of the stacked package to $\sim 20\mu m$.

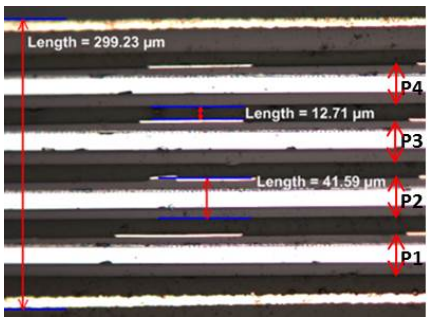


(a)



(b)

Figure 3.10: (a): Multi-UTCP panel (180 chip packages on a single panel) on alignment tool plates for stacking, (b) Schematic cross-section of the build-up of the lamination stack



(a) Stack cross-section: Chip region

(b) Stack cross-section: Off-Chip region

Figure 3.11: Cross section pictures of stack of 4 packages (P1-P4) of total thickness: (a) $\sim 300\mu m$ in the chip area, (b) $\sim 280\mu m$ outside the chip area

3.3.3 Laser Drilling for making THVs

After the lamination step, the interconnection within each layer of the UTCPs can be established by using though hole via (THV) interconnection technology, which includes via formation and via plating after-wards. The preliminary optimization test was made for making TH of 1:1 aspect ratio, i.e, $200\mu m$ via diameter on a stack of thickness $\sim$ $200\mu m$ (ref: Section 2.4.3 of Chapter 2). Those parameters are fine tuned in this demonstrator production process where the stack thickness is found to be $\sim 300\mu m$. Some more issues in this THV processing are listed below.

Misalignment issue (Figure 3.12-a):

Due to CTE mismatch between the polyimide PI 2611 ($3ppm/^{\circ}C$) and the carrier material (glass, $8.7ppm/^{\circ}C$), a linear shrinkage of $\sim$ 0.2% has been measured. This leads to the deformation in UTCP sheets when they are fabricated on large substrates (e.g, 4" or 6" glass carriers). Also the same deformation is retained within the stack after lamination. This results in misplacing the THVs. This deformation needs to be taken into account during the design phase.

Focusing problem (Figure 3.12-b):

As the stack itself is flexible, it does not stay flat on the carrier during the drilling process. This results in incomplete drilling through the stack due to lack of focusing at certain points.

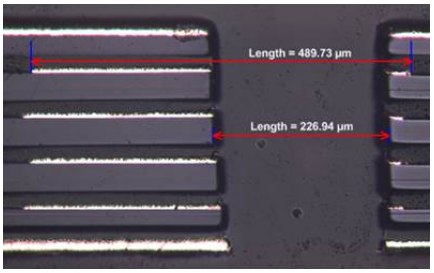
Undercutting within the stack (Figure 3.12-c):

The inhomogeneous thermal conductivity of each underlying layer and the shape of the laser beam influence the temperature and as a result the amount of ablated material. This implies that the laser parameters (pulses at a place, power) have to be optimized to minimize the local heating/ melting of the different layers which could lead to undercutting. Figure 3.12-c shows that LF 100 is sensitive to undercutting.

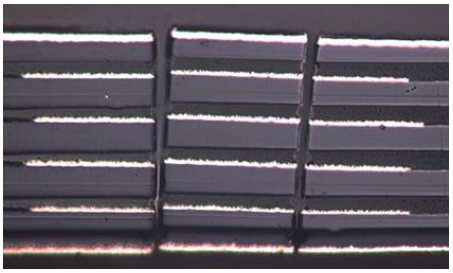
It has been reported that Laser pulses with uniform energies can be realized either by shorter duration of the pulse accompanied by higher peak power, or by longer pulse duration with lower peak power [52]. In the optimization of the laser drilling process, first the total number of pulses at one spot and the laser power were optimized for drilling the TH out of a stack of a specified thickness (usually $300\mu m$). Optimized laser drilling parameters for this process are given below.

- Laser Power (E) = 500 mW
- Pulse repetition rate (f) = 10 kHz
- Spot size of YAG laser (d) = $25\mu m$
- Pulses at a place (n_1) = 10
- Number of places per round (n_2) = $3.14 \times D/d$ (here D = Through Hole diameter= $200\mu m$) = 25

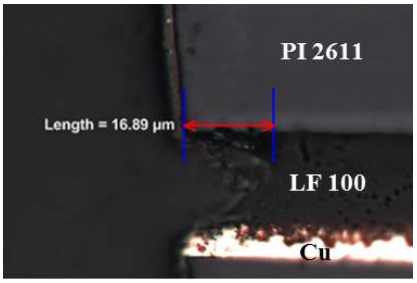
- Pulses per round (n_3) = $n_1 \times n_2$ = 250
- Total pulses at a place (n_4) = 400 (set for stack of $300 - 400\mu m$ thickness)
- Total round(n_5) = n_4/n_1 = 40
- Total pulses to drill one TH (N) = $n_3 \times n_5$ = 10000
- Round per sec (R) = f/n_3 (input parameters for trepanning) = 40



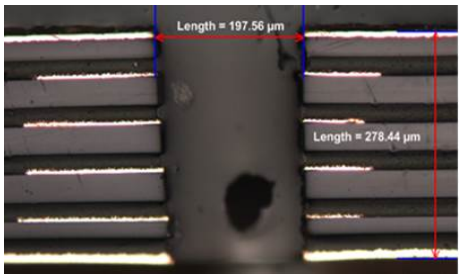
(a) $120\mu m$ shift in TH Position



(b) Focusing problem



(c) Adhesive undercutting



(d) Smooth THV wall

Figure 3.12: Cross-sectional view of the THV showing (a) misalignment problem ($120\mu m$ shifting): THV is not at the center of stack of contact pads, (b) focusing problem: via could not be cut through the stack, (c) undercutting problem: Acrylic material (LF 100) melting out under the polyimide layer due to thermal effect (d) smooth THV wall drilled with optimized set of laser parameters (Power $500mW$, frequency $10kHz$, Energy $\sim 500mJ$, time $\sim 1s$).

To minimize the undercutting of LF 100 within the stack, the local heating effect during Laser processing was investigated. Instead of giving the needed total number of pulses (n_4) = 400 at once, it is divided into shorter "salvos" (n_1) of 10 pulses each at a certain spot. As the trepanning process allows the rotation of the Laser to make a circle of desired TH dimension (here D= $200\mu m$), the total pulses at a place were delivered by making a number of rotations n_5 = 40. By choosing very small n_1 value, the rotation speed (R) increases which does not add much difference to the heating effect. After some intensive tests by varying the laser power and the number of pulses at a place per "salvo", a uniform TH profile (as shown in Figure 3.12-d) was realized

on the stack with following set of parameters. The top view of the panel containing matrices of stacks with through holes defined at the exact place is given in Figure 3.13.

The energy of 1 pulse of laser with power $500mW$ and pulse repetition rate $10kHz$ is calculated to be $50\mu J$. Assuming a spot size of the YAG laser equal to $25\mu m$, the laser fluence (Φ) can be derived as $10.19J/cm^2$. If the total pulses (n_4) given at a point for making through hole is 400, the effective fluence (Φ_{eff}) can be calculated as, $4076J/cm^2$. The Laser pulse energy used and time taken in drilling one TH of $200\mu m$ diameter on a stack of thickness $\sim 300\mu m$ are $502.4mJ$ and $1s$ respectively.

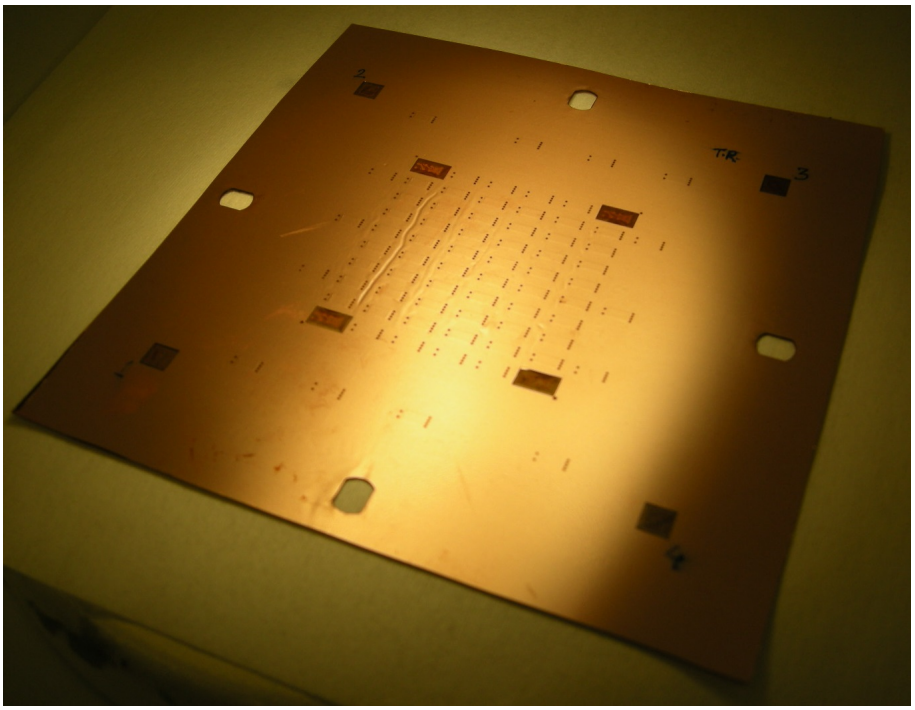


Figure 3.13: Top view of the panel containing matrices of stacks after drilling through holes

3.3.4 Desmear

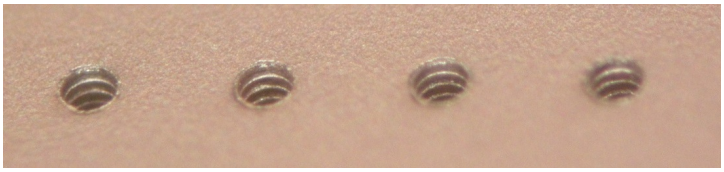
After repeated tests and the cross-sectional analysis of the TH wall (ref: Chapter 2), the RIE parameters for getting more or less debri free wall are set and given in Table 3.2. This 2 step RIE exposure is done both from top side and bottom side of the stack.

Table 3.2: Reactive ion etching parameters for desmear Process

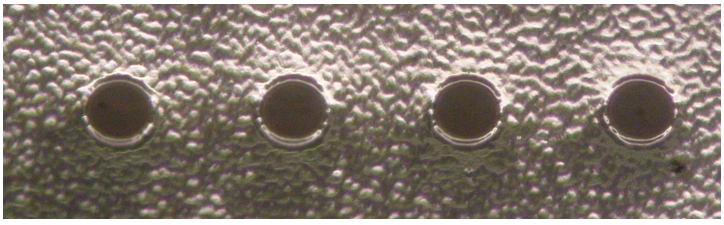
Step	Power	Pressure	Gas flow rate	Duration
	$watt$	$mTorr$	$sccm$	min
1	150	100	$CHF_3 : 5, O_2 : 20$	2
2	150	100	$O_2 : 25$	1

3.3.5 Metallization

The standardized set of parameters discussed in chapter 2 were used for initial metallization of the surface and through holes by electroless copper deposition and a subsequent electrolytic copper plating step. Electroless copper deposits a very thin ($\sim 2 - 4\mu m$), fragile coating of pure copper over the entire surface of the panel. This includes the drilled TH walls and external surfaces (top and bottom side of the stack). Electroplating then proceeded to increase the thickness of the copper to a final value of $10 - 12\mu m$. The top view of through hole made on the stack after electroless and galvanic Cu plating are shown in Figure 3.14.



(a) after electroless Cu plating

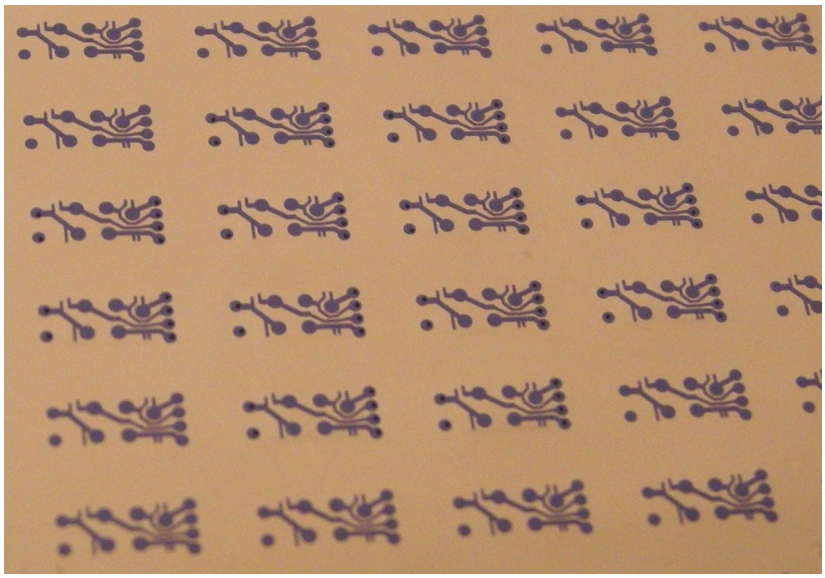


(b) after galvanic Cu plating

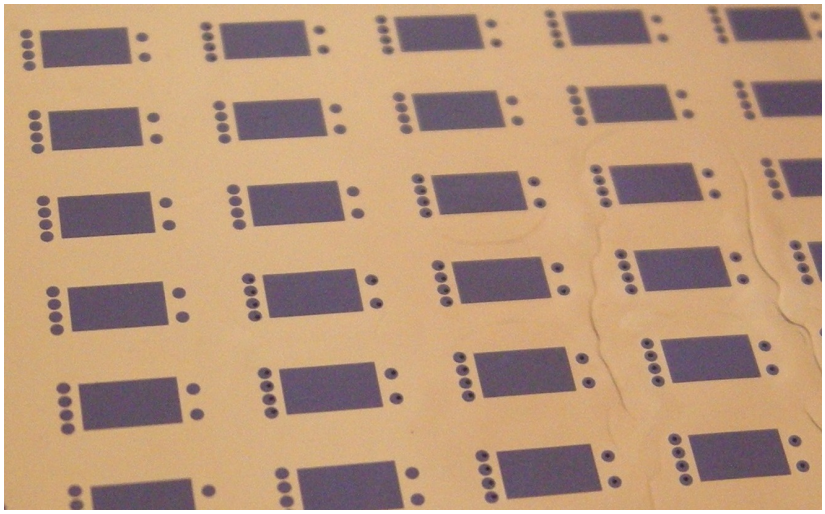
Figure 3.14: Top view of the through holes after electroless and galvanic Cu plating process

3.3.6 Patterning and dicing

The final Copper patterning is done on both top and bottom sides of the stack protecting the plated through hole and some fine conductive lines on the stack.



(a) Top side pattern



(b) Bottom side pattern

Figure 3.15: DFR pattern on the stack after development

Riston FX920, a $20\mu m$ thick negative Dry Film Resist (DFR) from DuPont Electronic Technology, is laminated on the both sides of the whole stack using a dry film laminator machine at a temperature $120°C$ with a speed of $0.85m/min$. Photo patterning was done both sides of the stack by illuminating the laminated stack by UV exposure with an energy of $63mJ/cm^2$, followed by peeling the protective layer

from the resist and developing it in 0.8% Na_2CO_3 solution. For better adhesion of the resist on the copper surface, a post development curing step can be introduced either by a baking cycle (at $120^{\circ}C$ in an air convection oven for $10 - 15min$) or by UV exposure ($100 - 150mJ/cm^2$).

The resist pattern on the top and bottom side of the stack is shown in Figure 3.15. After developing, the exposed Cu layer from both top and bottom sides of the stack is etched by a Cu-spray etching process in a $CuCl_2 \bullet 2H_2O + HCl$ solution at $55^{\circ}C$. Finally the resist stripping was done by stirring the stack in 3% NaOH solution ($55^{\circ}C$) for $3min$. This is an uniform etching process, used by almost all PCB manufacturing industries and is standardized set of parameters at our CMST group.

The final process is dicing of the whole panel which can be done by laser cutting by using the almost same set of parameters used for making the through holes (minus trepanning). Figure 3.16 shows the miniaturized modules after dicing them into individual stacks.

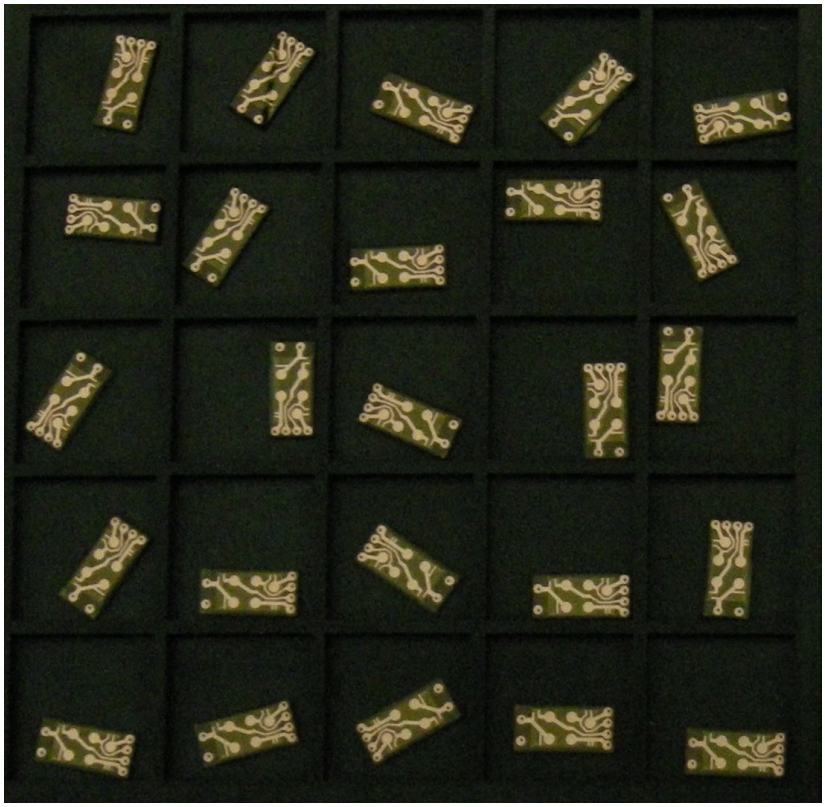


Figure 3.16: The diced stacks

3.4 Result

The whole process was realized in producing stacks containing four EEPROM dies of size $5.45mm \times 2.56mm \times 300\mu m$. Figure 3.17 shows a close view of embedded EEPROM dies and the interconnection pattern for package 1 (before release from the glass substrate) and the 3D-view of the diced stack.

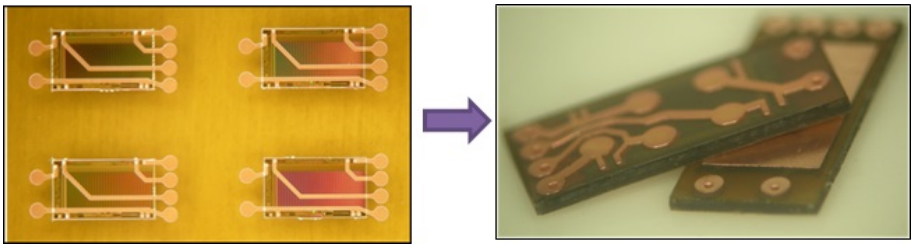


Figure 3.17: Left: Close view of Multiple UTCPs (this is picture only for package 1) fabricated on a single panel, Right: 3D view of EEPROM stack (4 dies with total stack thickness of $300\mu m$)

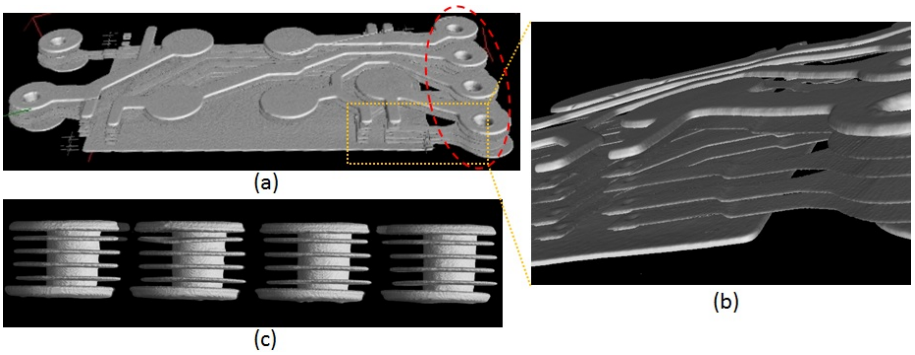


Figure 3.18: X-ray CT scan picture of one stacked UTCP showing (a) only conductive lines within the stack, (b) close-up view at the Cu routing from the chip contact pads to the TH pads (c) side view of the stack (red marked) illustrating vertical interconnection by through hole plating

Figure 3.18 is the X-Ray CT scan picture of the stack which is reconstructed from the 2D pictures taken at different angles by rotating the stack. The internal circuitry within the stack can be easily seen by this characterization technology. The figure below shows the snap-shots of the internal metallic structures of the stack taken at various angles of view giving a complete picture of 3D-interconnection via plated through hole.

3.4.1 Characterization

The connectivity of the chip packages is verified by checking the functionality of ESD pad protection diodes on the chips by 2 point measurement set-up. If the chip pads are well connected to the outside world, a typical diode impedance characteristic between the functional pads and the ground pads is measured. The $I \sim V$ characteristics shown in Figure 3.19 were drawn from this measurement result with P1: Ground and P2: Vcc as the contact points on the stack. The current was measured within the voltage range of $-1V$ to $+3V$ for all the stacks. Out of 11 stacks (as in the plot), only S1-S4 were proven to be functional and rest were non-functional as the current raises with voltage after $1V$ which indicates shorts in the circuit.

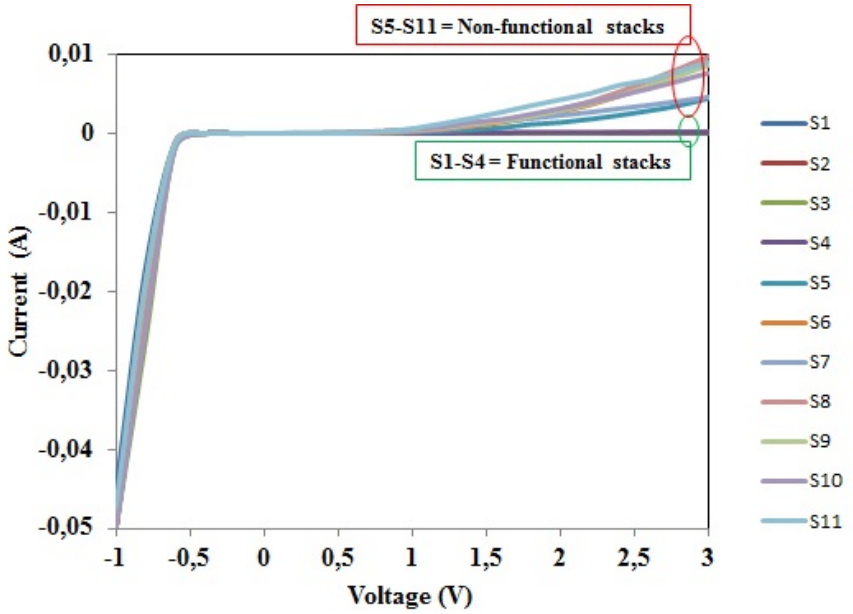
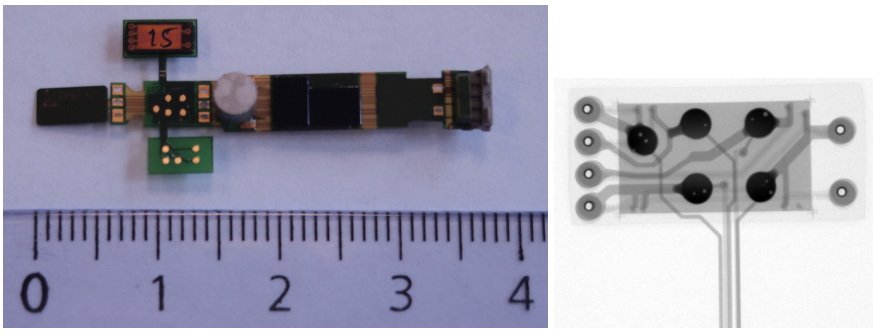


Figure 3.19: Top side view of the EEPROM stack with external contact points (left picture) with graphical representation of two point connectivity test result, measured at the points P1: ground and P2: Vcc of 11 stacks (S1-S11)

3.4.2 Mounting on Flex Circuit

The Oticon's Hearing aid device was one of the end product of TIPS project. The flex circuit used inside the device was designed by Oticon which contains place for 4 EEPEOM chips. This space for the 4 dies is preserved by use of this novel technology where vertical dimension plays the role of assembling memory dies. The stack containing 4 EEPROM chip packages has the thickness and size comparable to that of a single bare EEPROM die. This miniatuarized module is mounted inside the flex circuit (Figure 3.20) and finally encapsulated inside Hearing aid device to make it

fully functional. After making the complete process by use of EEPROM stacks, 2 of the devices were found fully functional (reported by Oticon in TIPS final review).



(a) Flex circuit used inside the hearing aid device, designed by Oticon

(b) X-ray picture of the stack after mounting it on the flex

Figure 3.20: (a) Flex circuit used inside the hearing aid device, designed by Oticon, (b) X-ray picture of the stack after mounting it on the flex

3.5 Failure Analysis

The average single chip packaging yield per each layout of UTCPs was $\eta = 83.5\%$. Problem in thin chip handling during chip placement (high pressure) and copper routing at the non-flat edge of the package are the main reasons for this minor loss in yield. During the mass production of these UTCPs, these errors cannot be avoided. However consequences on yield loss of the individual layers become more severe when these layers are stacked to form the 4-chip EEPROM stack. With the assumption that inclusion of a single non-functional package within a stack makes the whole module non-functional, the expected stack yield was calculated to be $\eta_u = 52\%$. This value can be theoretically interpreted as $\eta_u = \eta^n$, where n is number of packages per stack. In our experiment, the yield η_u was measured to be 46%. The schematic diagram illustrating the influence of single UTCP packaging yield on stack yield is shown in Figure 3.21.

After the complete stacking process, the yield per batch of stack turns out to be 7%. This value can be termed as $\eta_{eff} = \eta_u \times \eta_s$ which is the effective yield of whole process and includes both the yield factors of UTCP process (η_u) and stacking process (η_s). In the current process, η_s is calculated as $\sim 15\%$. During failure analysis based on cross-section of the non-functional stack, cracks at certain parts of chip were observed (Figure 3.22). These cracks were suspected to be the main failure cause of those stacks. This defect could have been introduced in any of the following processing steps: during thin chip handling, or during the stack lamination process.

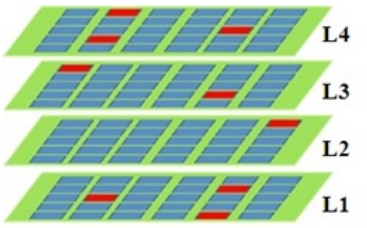
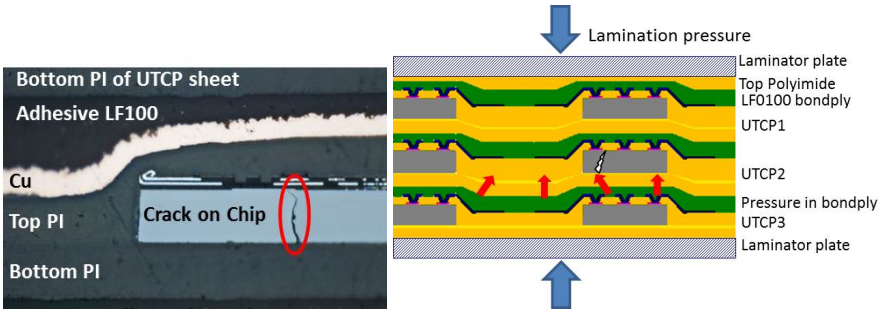


Figure 3.21: Schematics of batch stacking: red color symbolizes nonfunctional UTCPs per each layer of packages allowing to determinate the yield after stacking



(a) Cross-section of failed stack showing thin die cracking

(b) Lamination process being one of the probable reasons for introducing cracks in thin dies

Figure 3.22: (a)Cross-section of failed stack showing thin die cracking, (b) lamination process being one of the probable reasons for introducing cracks in thin dies

3.5.1 Analysis of die cracking

Thin chip handling

As described in section 3.3.1, the adhesive glue used for the chip placement and bonding on the base polyimide layer was PI2611. The experimental result by use of different types of polyimide as bonding material for the silicon chip bonding proves to be a bad choice because of the polyimide curing mechanism [21]. In this process, a lot of water is released as a by-product of polyimide [39] and chances of getting air trap under the chips cannot be avoided. Although the UTCP technology using PI2611 as adhesive glue is giving a high yield (average 83.5%) after fabrication, the presence of air under the chip becomes more critical in the subsequent high temperature and pressure processes like package-on-package lamination. A similar type of failure mechanism has been reported by [66] during the reflow soldering process in plastic LSIs. The moisture content within the package plays a significant role in the die cracking mechanism.

Once the void is trapped during the chip placement process, the sample has to go through different curing cycle and that generates a bending stress at the thin chip region. In the UTCP processing, the maximum curing temperature is $350°C$. As both the PI 2611 and Silicon chip have same CTE, the chances of crack formation due to this bending stress is minimum. In the lamination process, the maximum applied temperature and pressure applied on the alternate layers of UTCP stack are $195°C$ and $250N/cm^2$. The presence of a void under chip together with the applied pressure at certain temperature can be the reason of die cracking. This demands a void-free flat-chip bonding process instead of this bending stress in thin chip.

Lamination process

Another reason for this failure can be the non-uniformity in the package thickness at the chip edge due to the chip height and a minor fluctuation in package-to-package alignment ($\sim\ 20\mu m$) before lamination. This thickness non-uniformity plays an important role during the lamination process. When pressure is applied at the adhesive flow stage, the liquefied glue on the top of chip package squeezes out from the chip area leaving a very thin layer on the top of the chip (Figure 3.22-a). Also the combined effect of $\sim 20\mu m$ package-to-package misalignment and the package topography at the chip edge (Figure 3.22-b) results a non-uniform pressure distribution on the overall surface of the embedded packages. Therefore the pressure non-uniformity during the lamination process can be a reason for chip cracking. To overcome this problem of pressure non-uniformity, either the bondply has to be thick enough which can compensate this thickness non-uniformity during the adhesive flow stage or all the layers within the stack have to be flat enough before laminating.

3.5.2 Different Approaches to solve the issue

Pyralux LF 200 as adhesive material

The first approach has been experimentally verified by using $50\mu m$ thick adhesive film Pyralux LF 200 from DuPont Electronic materials [45] replacing the standard one, $25\mu m$ thick Pyralux LF 100 used in the above said fabrication process. In this experiment, the UTCPs were optically aligned by looking through stereo-zoom microscope on top of each other with the $50\mu m$ thick adhesive film in between. The top covering layer used here was $25\mu m$ thick polyimide film for the transparency in viewing the defect from top side (not by making cross-section of the stack). The lamination parameter used are the same which has been used for checking the adhesive flow test and peeling strength test (with respect to Cu and PI 2611) results.

The result of this lamination test is cited in the Figure 3.23 which is the top view of stack showing the uncured adhesive glue at the chip edge of the stacked packages. As per the Pyralux bondply datasheet [45], for the complete curing of the material a particular range of temperature and pressure most be applied. This implies the lamination parameter used here is not good enough for the bondply to compensate the height difference at the chip edge of the package which leaves the glue uncured

due to insufficient pressure at that point. Additionally, chance of die cracking may not be avoided by this process which can be verified from the Figure 3.23 showing crack on the top most embedded die of the stack. To get a better result, the whole lamination process has to be monitored with a close view on the adhesive flow step and applied pressure. Another disadvantage in solving the problem in this direction can lead to optimizing again the through hole drilling parameters as per the adhesive layer thickness to overcome the undercutting issue. Moreover the total stack thickness (considering 4 packages) will be increased by a factor of 25% by switching to thicker bondply ($50\mu m$ instead of $25\mu m$).

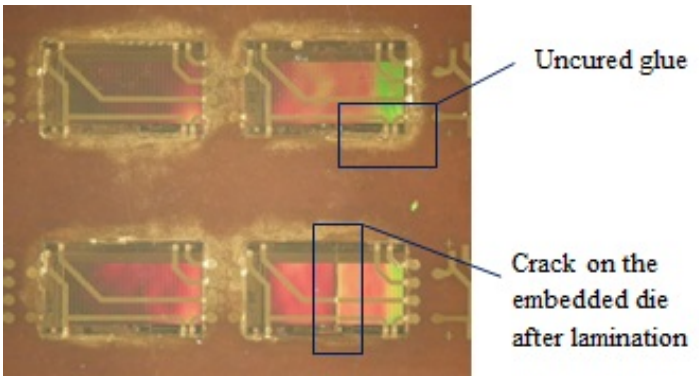


Figure 3.23: Top view of the laminated stack of non-flat UTCPs by using $50\mu m$ thick LF 200 as bonding material

Flat-UTCP Approach

Introducing an extra layer of polyimide can make the whole package flat enough which can solve this pressure non-uniformity issue. This additional polyimide layer has a thickness which is the same as the thinned dies in-between the base and top layers of the chip packages [28], [58]. The embedding capability in standard FPC's (flexible printed circuits) of individual Flat-UTCPs have already been demonstrated by IMEC in the past couple of years [28], [63], [64]. A recent development in this technology confirms 95% production yield by 3D-integrating this Flat-UTCP in standard flexible circuit boards (FCB) [28]. Taking the advantage of this developed technology and combining it with multi- thin chip placement process can improve the mass production process with high yield. The process development and the related issues for this Flat-UTCP approach is discussed in chapter 4.

3.6 Conclusion

A 3D-stacking technology based on conventional 2-polyimide layered UTCPs is demonstrated in this chapter. The average yield of UTCPs per panel is 83.5% and the yield after stacking four such layers is measured to be 46%. However the actual value is

found to be 7%. The major failure occurs due to die cracking during lamination process due to non-flatness at the chip edge of the conventional UTCPs. To achieve pressure uniformity during lamination process, all the layers within the laminated packages has to be completely flat. This also required flat-chip bonding on the base polyimide layer without air-trap. The development based on improving these two processes are discussed in the chapter 4.

Chapter 4

Photo definable Polyimide based UTCP concept

4.1 Introduction

The basic philosophy behind developing this technology is to make the whole package flat enough at the chip edge to prevent the shorts in the fan-out due to chip height. Additionally, flatness at the chip edge of the package can be good choice to overcome the die cracking issue during the package-on-package stacking process. The thin chip embedding technology used in the fabrication of 1st demonstrator production (Chapter 3) was based on 2-layered spin-on polyimide PI2611 which had a major failure issue due to non-flatness of the package. By introduction of an extra polyimide layer of thickness similar to the chip thickness can flatten the whole package. As a result it can solve the pressure non-uniformity issue in the stacked packages (Figure 4.1).

The technology development to produce flat ultra thin chip package (Flat-UTCP) in a large scale is discussed in this chapter. The concept of Flat-UTCP and some challenges in selecting the right material for this technology is discussed in the first section. This will be followed by issues related to fabrication process and redesigned process flow for multi-Flat-UTCPs production.

4.2 Flat-UTCP technology

In the past couple of years, our CMST group has done lot of development in this technology. This has been reported in many of the publications and conferences [28], [58], [63], [67]. The initial attempt (gen. 1) of fabrication and related issues are described in the PhD thesis of Jonathan Govaerts. A recent development on this technology (gen. 2) by solving those issues is reported in the PhD thesis of Liang Wang. The process development for large scale production of Flat-UTCPs by precise

placement of multiple thin chips on a single carrier and the related fabrication issues due to CTE mismatch are discussed in the current PhD work (gen. 3).

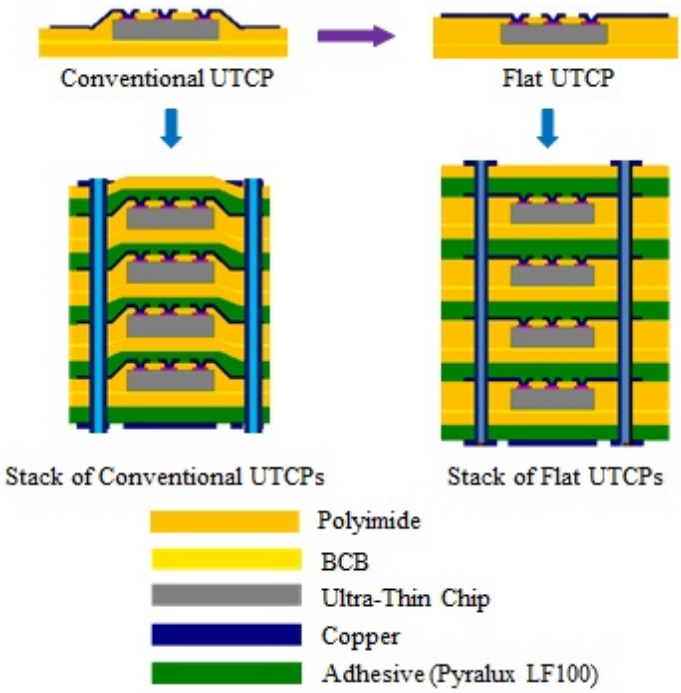


Figure 4.1: Schematic overview of stacking of Flat-UTCP approach

4.2.1 Flat-UTCP Technology (gen. 1)

This Flat-UTCP (gen. 1) has a symmetric build up with the use of two types of polyimides (non-photodefinable PI2611, Photodefinable PI, HD7012) from HD Microsystems. The different layers of polyimide in this structure are referred as base layer, the inner layer and top layer. Taking the advantage of photodefinable capability of PDPI HD7012, cavities of chip dimension are created on the inner layer. However this PI has a very high CTE ($70 ppm/°C$) as compared to other materials used in the package. By use of PI2611 ($3 ppm/°C$) both as top and bottom layer makes the whole build-up symmetric enough to avoid the curling of package after release from carrier due to CTE mismatch. Although the process of fabricating Flat-UTCP (gen. 1) is optimized [20], still there are lot of unsolved issues (listed below) which makes the whole process not reliable for mass production of Flat-UTCPs.

- Thin die handling during chip placement process
- Precise placement of thin chip within the cavity.

- Gap filling problem at the chip-cavity interface which causes difficulties in the materialization process (Figure 4.2)

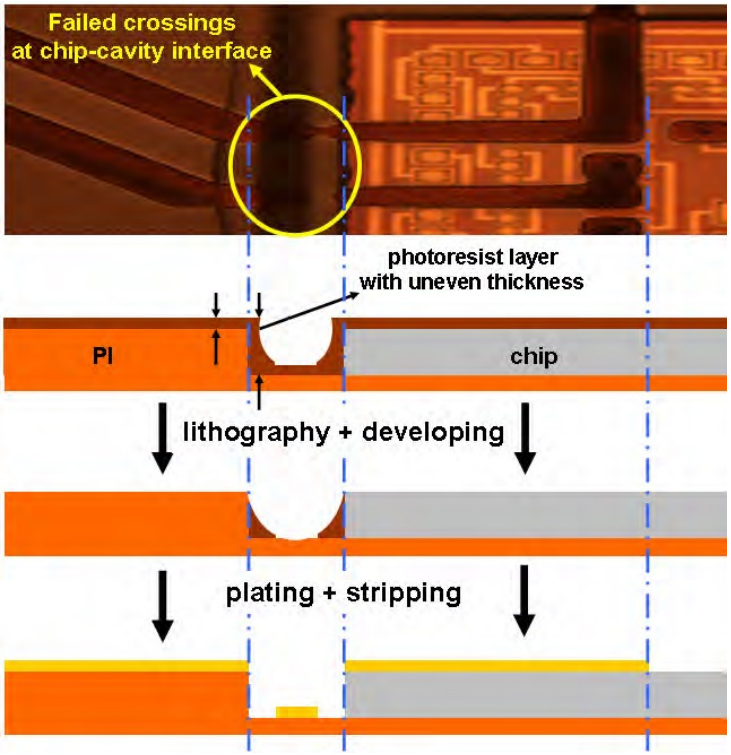
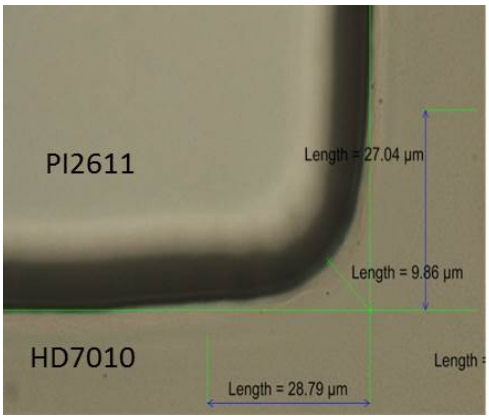


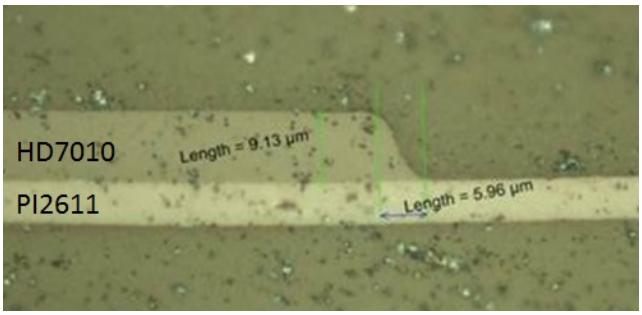
Figure 4.2: Bridging the gap at the chip-cavity interface [20], p-189

More investigation by using this set of polyimide build up was not possible as the company HD Microsystems stopped producing the PI HD7012. Some experiments were performed during the frame work of TIPS project to solve the gap-filling issue by replacing the inner layer by another photodefinable PI of same series (PDPI HD7010 [68]).

A chip with sharp edges cannot fit inside the cavity with having a corner curve and sharp wall slope (Figure 4.3). To overcome this issue, the cavity has to be considerably broader than the chip size. As a consequence, this difference in size causes gaps between chip and cavity wall. After some evaluation test of PDPI HD7010 processing, appropriate parameters are found to have the least wall slope width.



(a) Top view showing the cavity corner dimensions



(b) Cross-sectional view showing cavity wall slope

Figure 4.3: Cavity issues using Photodefinable PI HD7010 as inner layer

The chips are placed with $50 - 60\mu m$ precision within the cavity by using BCB as adhesive glue. Use of PI2611 both as bottom and top layer PI gives a symmetric structure, but is not sufficient to fill the chip-cavity gap (Figure 4.4-a). Applying PDPI HD7010 as top layer fills this gap more efficiently (Figure 4.4-b). But at the end, the package becomes unsymmetrical which results in curling of the polyimide layers after release from the carrier. More research on this process could not be continued as the production of PDPI HD7010 by HD Microsystems was terminated.

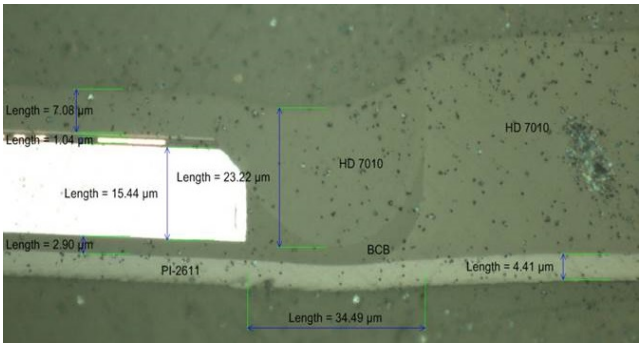
4.2.2 Flat-UTCP Technology (gen. 2)

The type of Polyimide used for this Flat-UTCP (gen. 2) fabrication is photodefinable polyimide HD4110 [40] from HD microsystems. This polyimide precursor was chosen for its following set of advantages.

- Self-priming property on both glass and Silicon: no adhesion promoter is required before applying it onto the carrier material and/ or silicon chip.

- Thickness range $8 - 20\mu m$: Easily tunable thickness by selecting appropriate spinning speed to achieve the desired thickness by a single spinning and curing step.
- Negatively photosensitive: Advantage in making self-aligned cavities for thin chips in Flat-UTCP fabrication process [69]. Additionally, micro-via realization on the contact pads of many chips well-aligned on the carrier can be done by a single lithography step on the covering polyimide layer [19].

(a) Gap filling capability of PI2611



(b) Gap filling capability of HD 7010

Figure 4.4: Cross-sectional view of at the chip-cavity interface showing gap filling capability by using different top PI layers

In the 1st stage of this development work, a flat chip placement on the base PI layer (HD4110) and photo-via technology by use of this PDPI HD4110 as top layer are developed [19]. Flat-UTCP technology (gen. 2)) with 3 layered polyimide build-up is developed in the subsequent stage. The cavity issues discussed in section 4.2.1 is solved by making self-aligned cavity. In this case, the thin chip bonded on the base-PI

layer is used as a self-aligned mask for making cavity in the inner/ flattening PI layer [69]. The result by introducing this novel approach improves the flatness of the the package at the chip edge. Figure 4.5 shows the conductive track topography at the chip edge which is wavy and straight for the case of non-flat and flat packages, respectively.

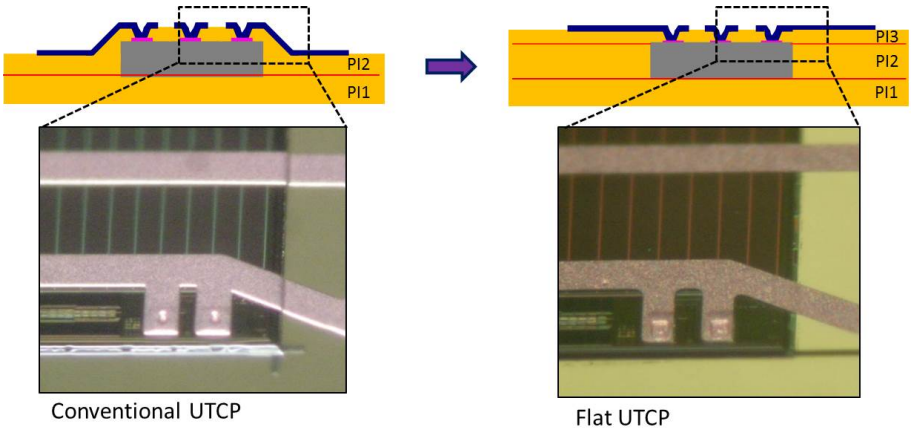


Figure 4.5: The transition from conventional UTCP to Flat-UTCP (gen. 2) showing the improvement in via structuring on the contact pads of EEPROM memory die and non-uniformity in the package thickness at the chip edge.

However, the process was developed for single UTCP per substrate where the precise placement of chips is not addressed.

4.2.3 Flat-UTCP Technology (gen. 3)

In the previous sections, the technology development is discussed for producing the Flat-UTCPs in lab scale (research level) where they are fabricated on 2 " glass carrier. For research on stacking of these package, the UTCPs should be fabricated in industrial level. This needs the packages to be processed on the carriers of large dimension, e.g., 4 " or 6 " or higher. The points of concern in this process are listed below.

- Selecting right set of Polyimide material to avoid the curling effect after release from the carrier due to CTE mismatch
- Deformation or shrinkage in the package due to CTE mismatch between base Polyimide and carrier.
- PI-PI adhesion if different sets of polyimide are used for reducing this deformation.
- Spacing between chips (max-min) for out of plane deformation control.
- Precise placement and bonding of multiple chips on a single carrier.

All these issues are addressed in great details in following sections. This will be followed by redesigning the process flow by introducing extra steps for the mass production of UTCPs.

4.3 Process flow for multi-Flat-UTCP (gen. 3)

The basic process flow for producing multiple Flat-UTCPs on the carrier of large dimension (e.g., 4 " or 6 ") is given in schematic diagram, Figure 4.6. The photodefinable polyimide used in this process is HD4110 which has a CTE of $35 ppm/°C$. This value is higher as compared to the other materials used in the package, including the CTE of substrate (glass) during fabrication process. The room temperature linear CTE and Young's modulus of these materials used in the UTCP fabrication process are listed in Table 4.1.

Table 4.1: CTE and Young's modulus of different materials used in UTCP

Material	Thickness (μm)	CTE ($ppm/°C$)	Young's Modulus (GPa)
Glass(white float)	700	8.7	70 ± 2
Glass(Borofloat)	500	3.7	64
PDPI HD4110	15-20	35	3.3
Standard PI2611	$5 - 15$	3	8.5
BCB (cyclotene 3022-46)	2-3	42	2.9 ± 0.2
Silicon Chip	20-30	3	130-185
Copper	7-8	17	117

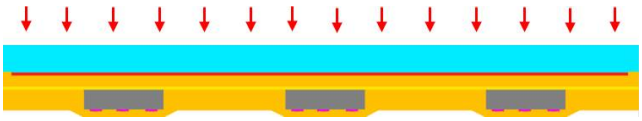
The effective CTE of the composite containing different layers of materials can be calculated from the Schapery Equation [70]. This takes into account the CTE values of the individual components of the composite, the volume fraction, the Young's modulus of elasticity and Poissons's ratio of each component. Assuming the Poisson's ratio of all the materials to be nearly of same order, it can be neglected in this equation.

$$CTE_{eff} = \frac{\sum_{i=1}^{n} CTE_i \times Y_i \times V_i}{\sum_{i=1}^{n} Y_i \times V_i} \tag{4.1}$$

where, CTE_{eff} = Effective CTE of the composite,
CTE_i = CTE of individual material in the composite,
Y_i = Young's modulus of elasticity,
V_i = Volume of individual material.

(a) Step 1. Spinning PDPI HD4110 on glass carrier with alignment mark and release layer

(b) Step2. Precise placement and bonding of multiple chips on the base PDPI layer by using spin-on BCB as bonding material



(c) Step3. Spinning of flattening PDPI layer and backside illumination through the transparent carrier

(d) Step4. Self-Aligned cavity for chips after PDPI development

(e) Step5. Microvia opening on covering PDPI by Photolithography

(f) Step6. Metal deposition and patterning

Figure 4.6: Process flow for producing multiple Flat-UTCPs on a single carrier

The polyimides (HD4110 and/or PI2611) and carrier (white float or Borofloat glass) used for UTCP fabrication are of different CTE. Making a right combination of materials is a matter of concern which can affect the package release process together with overall deformation in the package after release.

4.3.1 Issue 1: Package release process

The self-priming property of PDPI HD4110 makes it a good candidate for direct adhesion on the glass carrier without use of any primer. For the release of package from the carriers, a salt based release technology is used [19]. The substrates are wrapped by Aluminium foil (shadow mask) covering the edges upto $\sim$ $5mm$ before loading them into vacuum chamber. This results in selectively evaporated of

thin layer of salt ($\sim$ $500nm$, KCl) only on the central part of the substrate. After spinning the base PI layer over the salt layer, the PDPI adheres well only at the edge of the carrier and has a moderate adhesion at the central part where the salt is deposited. After the complete UTCP process, a precise cutting at the edge of the package is made and the substrate is immersed inside DI water. This facilitates water to enter underneath the package to dissolve the underlying salt for easy release of package.

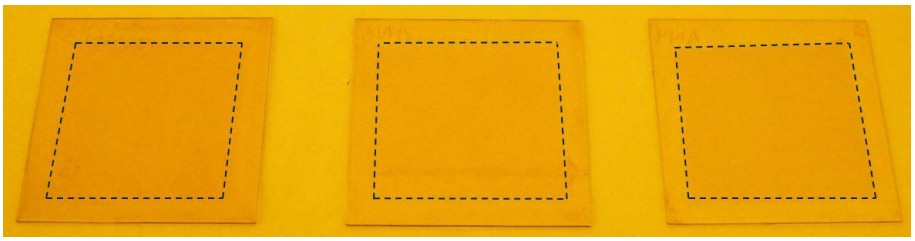
A similar process can be implemented for an easy release of the package with PI2611 as base layer. In this case, a primer VM652 [43] from HD Microsystems is applied at the edge of the carrier before spinning the base PI layer as this PI has a bad adhesion on the glass.

The current UTCP process includes a number of wet process along with salt as release layer. It has been experimentally proven that PDPI HD4110 is more prone to water uptake that its counter part, standard polyimide PI2611. Using PDPI HD4110 as the base PI layer sometimes makes it difficult to process it in large substrate. It adds the risk of pre-fabricated package release. The maximum number of 4 " carriers that can be loaded in evaporation chamber (Leybold-Heraeus Univex 450, in Cmst clean Room) for salt evaporation is 4. For continuing experiments on package deformation and release, more number of samples with release layer are required. To gain more knowledge on the different PI combination, all the experiments are performed on 2 " carriers in stead of 4 ".

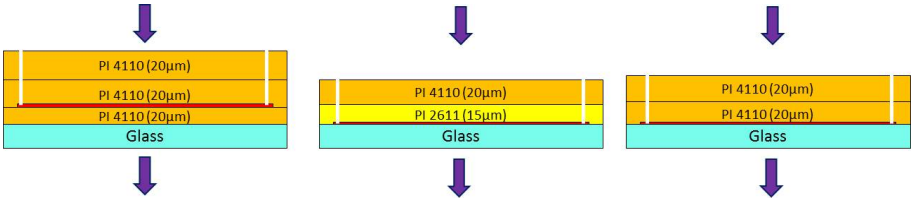
An experiment was conducted by use of different combination of PI (only top and bottom layer) to evaluate this release process. As shown in the Figure 4.7 (2nd option), by making the cut at the PI, the stack of PI curls like a cigarette in the direction of high CTE PI.

The 3rd option shows the stack of 2 layered PDPI layer spin-cured directly on glass with salt as release layer. After precise cutting at the edges, it pops off automatically from the carrier and stays flat afterwards. If a chip is embedded within the PI, the chance of thin chip cracking cannot be avoided in this type of release process.

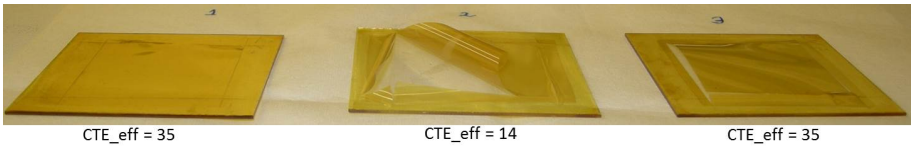
When the glass carrier is spin coated by same PI (PDPI HD4110), the package stays flat on the carrier even after complete cutting of the central part (1st option). In this case, the effective CTE of carrier (glass + PDPI HD4110), calculated by Schapery equation (Eqn. 4.1) is different than that of only glass which is more convenient for the smooth release of PI stack. But the disadvantage is it will add an extra PI spinning and curing step to the whole process flow. Also curling of entire sample has been noticed when more layers of these PDPI HD4100 are applied on the carriers of larger dimension. This makes the fabrication process difficult which includes substrate mounting on vacuum chuck for making alignment (step 5 and 6, Figure 4.6).



(a) PI stack on the carrier before release



(b) Schematic cross-section of the PI stack on the carrier with cut made at the edges for release process



(c) Release of PI stack from the carrier (effective CTE of the released stack as calculated from Schapery equation)

Figure 4.7: Release of PI Stack from the glass carrier by salt based release technology

4.3.2 Issue 2: Package deformation control

To avoid curling of the package after release from carrier, the package should have a symmetric build-up. This means top and bottom layer PI should be of same material and of almost same thickness. A three layered PI build-up using PDPI HD4110 can solve the above said issues related to package symmetry. Due to high CTE difference between the carrier and PDPI material, after complete processing of package on the 4" glass substrate, a linear shrinkage of $\sim 0.9\%$ has been observed (Figure 4.8).

The calculation was done by measuring the distance between two extreme alignment marks on the package before and after release from the carrier. Before release, the value is same as that on the mask design and after release, the value lowers due to deformation in package. This is a very high value for the stacking technology where package on package alignment is done mechanically by making laser assisted pin holes (Chapter 3, Figure 3.8). The pin holes are made at the corner of the PI sheet before release of package from the carrier and they shifts from the desired position due to this shrinkage

in package. Finally, the polyimide film tears at this pin hole points when stretched to fit inside the lamination tool and as a result, the package-to-package alignment is lost by this process.

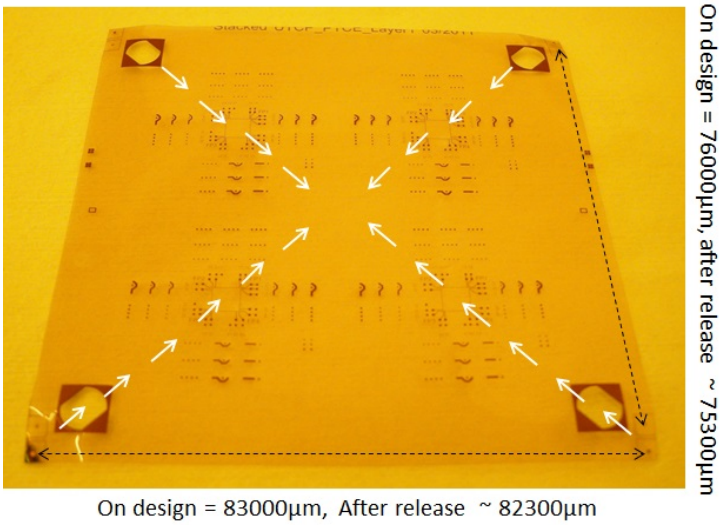


Figure 4.8: A released package (without chip) with copper pattern showing linear shrinkage of $\sim 0.9\%$

To overcome this issue, the deformation in package after release from the carrier has to be lowered. This can be achieved by any of the following ways.

An option can be use of both carrier and base PI of almost same CTE material. The conventional carrier material for the UTCP packaging is white float glass. The best suited polyimide precursors used for UTCP fabrication in our group are PI2611 and HD4110. The CTE of these 3 materials are drastically different from each other (see table 4.1). In section 3.3.3, a linear deformation of 0.2% has been reported for the PI2611 based UTCP fabricated in conventional process. A combination of these two PIs can resolve this issue by lowering the deformation level. A similar concept of stress balancing multilayer is being studied to control the out-of-plane deformation in MEMS fabrication process [71].

$$\Delta L/L = \Delta T \times \Delta CTE \tag{4.2}$$

where, L = Linear dimension of the package,
ΔL = Change in package dimension after release from carrier,
ΔT = Difference between PI curing temperature and room temperature,
ΔCTE = Difference between effective CTE of the whole package derived from equation 4.1 and CTE of the carrier.

An experiment has been conducted to evaluate the deformation by using different combinations these PIs. In this test, $20\mu m$ thick PDPI HD4110 is used as cavity layer and standard PI2611 of different thicknesses is used as top and bottom layer. The released package with the schematic cross-section showing layer thickness is cited in Figure 4.9. It can be seen that package with symmetry (same top and bottom layer thickness) has less curling effect than the one with uneven symmetry. However the linear shrinkage in both the cases are the same which is of $\sim 0.23\%$. This value is very close to the corresponding value for only PI2611 based UTCPs which is equal to 0.2%. The approximate value can also be calculated by using the Schapery equation (Eqn. 4.1) for effective CTE of the package and following equation 4.2.

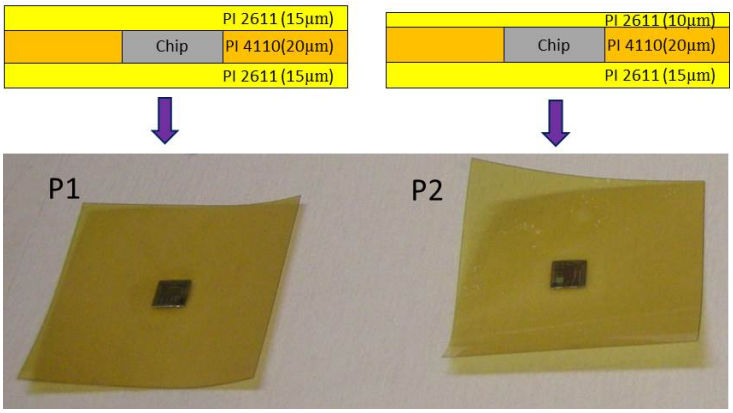


Figure 4.9: Released package with different PI thicknesses shown in schematic cross-section

Before using these two different PIs for the production process, it is necessary to study the PI-PI adhesion. Due to the self-priming property of PDPI HD4110, it adhere well on the glass and silicon material. Also a good adhesion of PDPI HD4110 spin coated on PI2611 has been verified by peeling test. This implies using PDPI HD4110 as cavity layer over the PI2611 is possible without any adhesion problem. However the adhesion of PI2611 spin-cured on PDPI HD4110 is comparatively poor. This difference in adhesion property within different layers of PI is not good for package reliability.

Additionally, laser ablation or reactive ion etching for via processing is necessary for opening vias on the covering PI which is not so fast and accurate as compared to the photo-via process. During the PhD of work of Liang Wang, the photo-via processing on PDPI HD4110 is optimized to generate micro-via down to $30\mu m$ [19]. If PDPI HD4110 is used as the top layer to overcome the issues related to adhesion and micro-via processing, the symmetry within the package will be lost. And the package with curl in the same way as shown in Figure 4.7 (2nd option).

With all these puzzles in the process, the preferred way to proceed is to use 3 layered PDPI HD4110. Package fabrication on large substrate (e.g., 4 " square white float glass) using this PI is difficult as the carrier itself curls up due to internal stress. This makes it quite difficult to handle the sample during alignment for via processing (Figure 4.6, step5) and even more problematic during metal patterning (Figure 4.6, step6). To reduce the stress during and after processing, some modification in design and process can be included.

To solve this CTE mismatch issue, some stress-relief patterns on the PDPI itself can be generated. This can reduce the internal stress upto certain extent which is induced after the polyimide curing process. This pattern can be created on the flattening and top PDPI layer during the cavity and via processing step, respectively.

Another effective way is to increase the silicon area within the package by inserting some dummy silicon chips which can lower the effective CTE of whole package by following Schapery Equation (Eqn. 4.1). This needs to be verified experimentally before proceeding in this direction.

4.3.3 Introduction of Stress-relief patterns in the PI thin film

The goal of making this pattern is to divide the polyimide layer with internal stress (due to higher CTE compared to carrier) into small areas. This in turn helps in localizing stress per package, instead of per panel. As a result, the deformation level per panel can be lowered after release from carrier.

These patterns can be fabricated on both flattening and covering polyimide layers where as the bottom layer has to be intact with the carrier without any pattern during the whole process. To reduce the cost of mask making, these patterns can be designed together with alignment pattern for precise placement of chip. It can be easily transferred on to the glass carrier by sputter deposition of a $50nm$ thick TiW layer and patterning it by wet chemical processing. The transparent carrier with the alignment patterns on it plays the role of mask during the backside UV-illumination process (Figure 4.6, step3). As a result, the same pattern gets transferred to the flattening layer polyimide film as stress-relief grooves. The metal pattern used for the chip alignment stays hidden under the thin-die and chip itself, act as a dark mask for making self-aligned cavities.

By using the same stress-relief pattern on the via mask, this can be easily transferred onto the covering PDPI film. As a consequence of this whole process, it will give rise to pseudo-islands of single UTCPs on the panel of multi-UTCPs.

4.3.4 Multiple thin Chip placement and complete bonding

Assembly of multiple thin chip is an necessary requirement for low cost micro-fabrication applications. Self-assembly of components [72] is a smart concept which

is now a topic of research at the current stage. A group in TU Delft is working self-assembly of ultra thin chip on flexible polymer by use of patterned magnetic field [73]. A combination of electrostatic fields and mechanical traps can be used to self-align the thin chips on a carrier wafer [74]. Laser Assisted Die Transfer [75] is one of the contact-less die transfer processes and it is based on Laser-Induced Forward Transfer (LIFT) [76] technology. All these processes are very fast, takes less than minute per multi-chip placement or transfer. However they have not reached the demand of industrial process where the component placement accuracy should be at least $\pm 35 \mu m$.

Multiple thin chip bonding together with void-free, flatness and accuracy in placement are the unavoidable issues for the mass production of UTCPs. The ulta-thin dies are very fragile and can be easily damaged during manual handling [35]. The pick-and-place equipment used for direct chip attachment cannot solve this issue successfully. Also, the die warpage can interfere the image-recognition system of the equipment. Some industries rely on this conventional way by use of flip chip die bonders with adapted tooling and special release tapes [55], [77]. Temporary carriers may be used to support the thinned dies during assembly [36].

As discussed in die cracking analysis section 3.5.1 in Chapter 3, the adhesive glue for chip bonding used in the UTCP process was PI2611. This has been reported by [21] to be bad choice for this application due to the polyimide curing mechanism. As per the bonding strength experiment [78], benzocyclobutene (BCB) from Dow chemicals is best suited for a void-free Silicon wafer bonding with homogeneous bonding strength. Cyclotene 3000 series from Dow chemicals [44] is being used by many researcher in our group [18], [19] for flat, air-trap free thin chip bonding [19] on polyimide surfaces. The issues related to thin chip bonding with placement accuracy are going to be discussed in this section.

Void-free flat Chip Placement

Dr. Tresky's semi-automatic Flip-chip bonder [79] used in our Group (Figure 4.10) has the capability of placing the components with an accuracy of $\pm 5 \mu$. However, the value differs when it is implemented in the UTCP processing. This includes Face-up placement of thinned dies on the pre-baked BCB, dispensed or spin-coated on the PI substrate.

The die handling tool having some structures for vacuum suction leaves its impression on the chip after the placement process. It can be seen by the surface profile analysis of the chip placed on a carrier (Figure 4.11-d). Some intermediate layers between the chip and the pick-up tool can be used for getting flat chip with no deformation. It is necessary to heat the underlying BCB up to $150^{\circ}C$ for the temporary die attachment onto the PI substrate. As the set-up consists of heating coil only around the chip pick-up spindle, the temporary carrier for chip or the intermediate layer has to be thermally conductive.

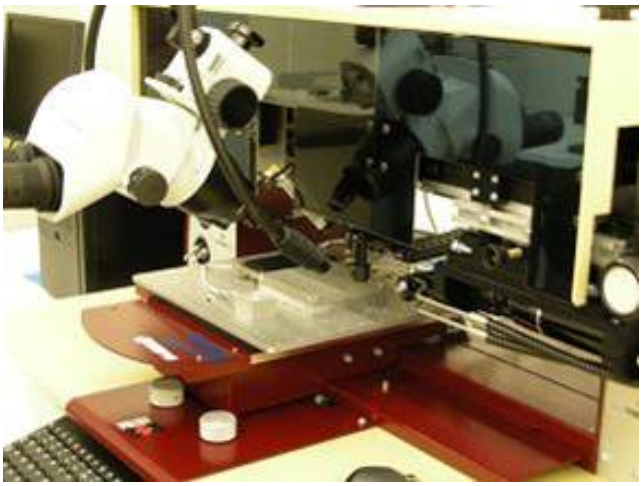


Figure 4.10: Dr. Tresky's semi-automatic Flip-chip bonder as installed in our Cleanroom

Some experiments were performed by using different intermediate layers (stencil steel, silicone tape and combination of both). Stencil steel (rigid material) having lot of tiny holes can apparently reduce the deformation in the thin chip. And silicone tape is a soft material which can avoid the chip cracking during the pre-bonding process. But the result was not reproducible in all the trials. The reason is non-flat pick-up tool and structures on the intermediate layers (or temporary carrier) which causes void under chip and imprint on the chip, respectively. After bonding 4-5 chips, it is advised to check the planarity of the pick-up tool. Making the tool flat is a time consuming step as the whole programme has to be restarted after doing this adjustment.

To avoid the problem caused by stencil steel (flat carrier with tiny holes which leave its impression on the thin dies), a rigid silicon or a glass with silicone tape glued on one side can be used as a temporary carrier for the chip. The thin chip (Face-up) can be directly attached to a silicone tape by electrostatic force and also it stays flat in the entire alignment process. The glass + silicone tape + thin chip can be picked together by vacuum suction and placed on the desired location after making alignment. The alignment can be made by using the flip-chip programme in the machine where the backside edge of the chips and the alignment pattern on the substrate are matched by the image-recognition system.

However at some instances some scratches on the contact pads can be visible by optical microscope (Figure 4.12-a). This is because of mishandling (accidental flipping of thin chip on the donor carrier) the during placement. This results in damaging the gold layer at certain parts of the contact pad which has been confirmed by SEM analysis (Figure 4.12-c). The donor carrier (glass or ceramic) has to be protected by some smooth material (Teflon sheet) to protect the thin chip from getting damaged.

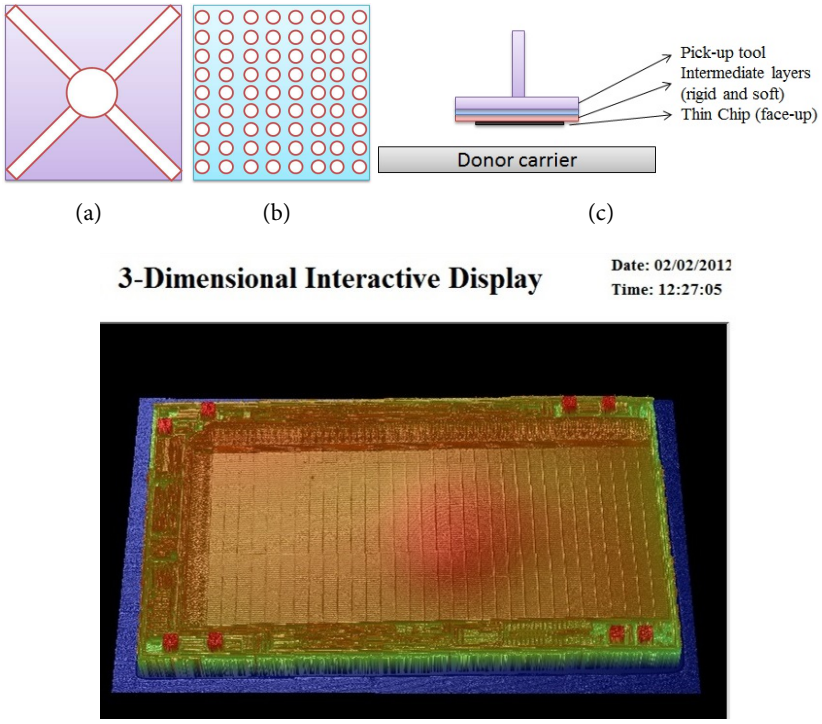


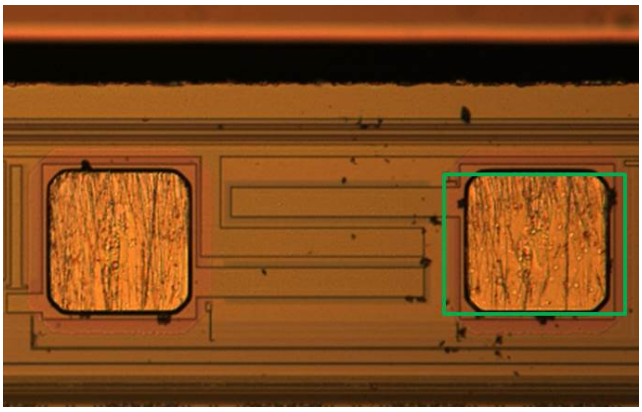
Figure 4.11: The schematics pick-up tool of Tresky (a) Front side pattern on the pick-up tool for vacuum suction of the chip, (b) Stencil metal (rigid) with having many tiny holes for vacuum spreading, (c) Chip being carried by the Tresky pick-up tool with two intermediate layers, (d) Surface morphology of the EEPROM chip studied by Wyko (optical profilometry) shows round elevated structure as an impression of vacuum chuck

Placement Accuracy after transfer

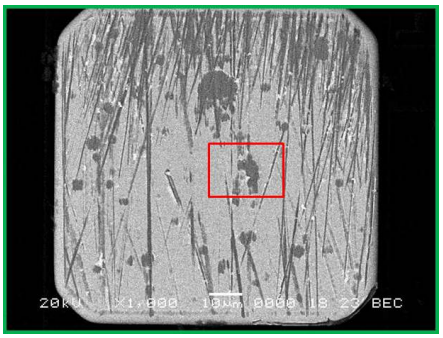
The risk factor in this process is the accuracy in the chip size after dicing. Before designing the alignment structures, this variation in size has to be taken into account. As the alignment is done via looking at the back side edge of the chip, a minor difference in diced chip size can lead to misplacement of the active area of the chip. It becomes more critical when the bond-pad size and pitch are of lower order ($< 50\mu m$).

After making the backside alignment, the chip is transferred to the substrate and pre-bonded on it by adhesive layer (BCB) spin-coated on it. The BCB under the chip can be heated for some time with an applied pressure on the chip. This is a requirement for die attachment and easy release from the temporary carrier.

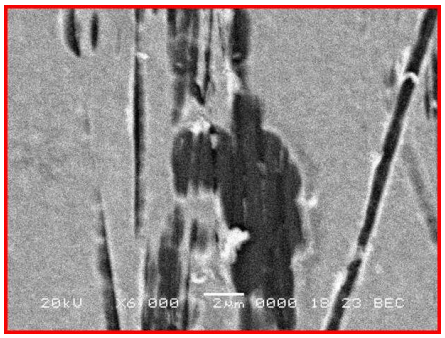
All the parameters like applied pressure per die, temperature and bonding time were optimized for flat die bonding on the PI film. The chips used for these experiments are of different size ($2.5\times2.5mm^2, 2\times3.5mm^2, 5\times5mm^2$) and thickness ($20\mu m, 30\mu m$).



(a) Optical microscope view of the contact pads



(b) SEM analysis of one of the contact pads



(c) zoom in to one point showing depression in the layer due to scratch

Figure 4.12: Microscopic analysis of the damages made on the thin chip while handling (a) Optical microscope view of the contact pads, (b) SEM analysis of one of the contact pads, (c) zoom in to one point showing depression in the layer due to scratch

BCB curing process with placement accuracy

The temperature and time parameters for the complete curing of BCB is given Figure 4.13. For good bonding strength, the applied pressure should be in the range of $1.7 - 2bar$ during the curing process [78]. The top surface has to be protected by covering layer before applying any load on the top.

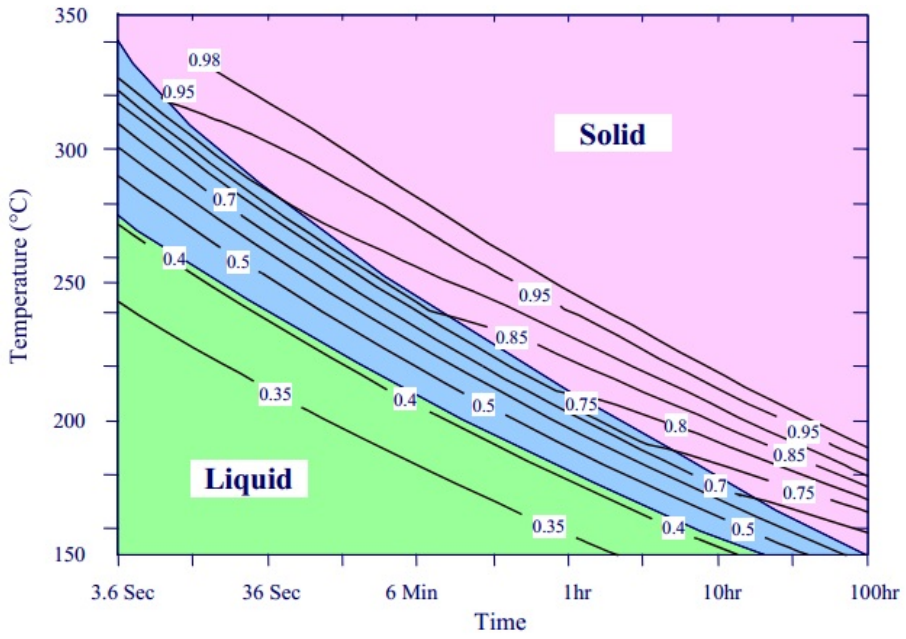
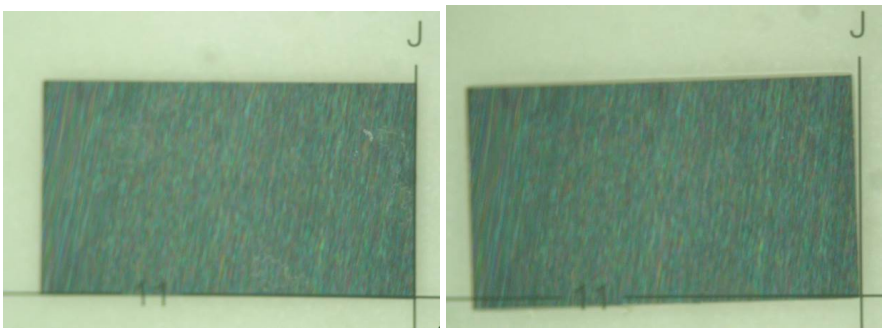


Figure 4.13: Different phase of BCB curing process as a function of temperature and time [44], where the indicated numbers in the plot shows the fraction of solid content in the total volume of BCB

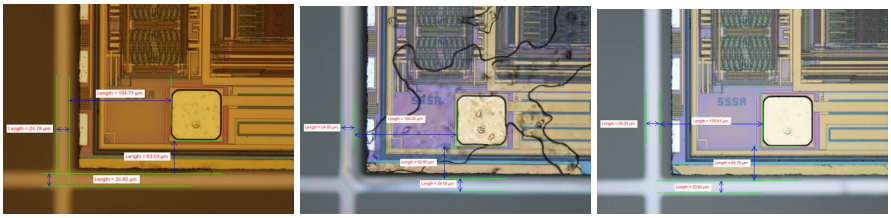


(a) (b)

Figure 4.14: Backside view of chip (a) after precise placement by Fine placer Tresky (b) after BCB curing process showing shifting of thin dies.

During the heating phase from ambient to curing temperature, BCB gets liquified and and finally solidifies when cured for longer duration. The BCB thickness under the chip is of the order of $3\mu m$ which is almost 10 times smaller compared to the chip

thickness. Due to applied pressure from the top of chip, the liquified BCB comes over the chip surface covering the contact pads and solidifies after the complete curing cycle. It is hard to clean the cured BCB film from the chip surface without damaging the underlying PI substrate. Additionally, the chance of chip movement in the liquid state of BCB is not avoidable (Figure 4.14).



(a) (b) (c)

Figure 4.15: One corner of the EEPROM chip (a) after prebonding of chip on the substrate by BCB (b) BCB overflow on the chip after precuring at $150°C$ for $30min$ (c) After wiping out the top surface of the chip by acetone

Following the curve given in Figure 4.13, the whole curing process can be divided into 3 parts to control this BCB overflow issue. This includes pre-curing in liquid phase to evaporate most of the solvents, half-curing in semi-solid phase and finally full-curing to reach solid phase.

At the 1st stage, the BCB is pre-cured at $150°C$ for $30min$ with a Teflon sheet covering the chip surface and an applied pressure of $1bar/die$. As per the phase diagram, it stays in liquid state at this elevated temperature. Due to the porosity in the Teflon sheet, BCB overflows cannot be prevented completely. Once the sample is cooled down to room temperature, the BCB over the chip surface can be cleaned up by gently wiping it by acetone. The placement accuracy after the cleaning phase has found to be retained after the cleaning step (Figure 4.15).

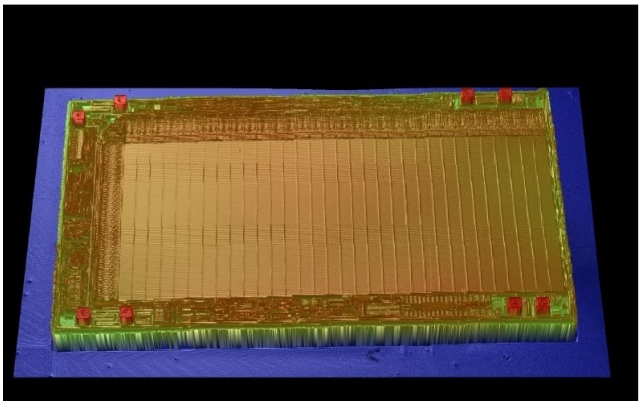
In the 2nd stage, the BCB is half-cured at $210°C$ for $30min$ with an applied pressure of $1.7bar/die$. The BCB turns 50% solid by end this temperature cycle. A very little chance of its overflow can be cleaned up by acetone wiping at room temperature.

The 3rd stage is to full cure the BCB in Nitrogen environment(as per the specification in [44]). This is the final bonding of chips onto the PDPI substrate which needs a pressure of $2bar/die$ and BCB curing at $260°C$ for $1h$.

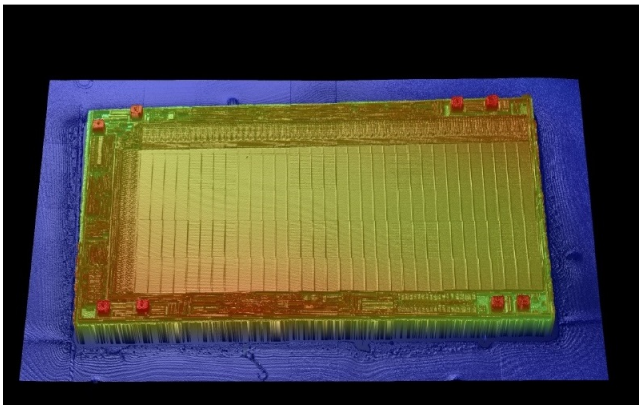
The chip placement and bonding process includes several intermediate steps and materials. It is necessary to check the chip position with respect to alignment mark and its surface (planarity and cleanliness) before going to the next step. The surface topography of the one EEPROM chip placed and fully bonded (by BCB curing) using

optimized set of parameters is shown in Figure 4.16.

The cleanliness of the chip surface (specially the contact pads) are verified by SEM analysis (Figure 4.17). No residues of BCB or silicone are noticed after the complete bonding of thin chip on the PDPI surface. This has been confirmed by EDX analysis of the top layer at certain parts of the contact pad.

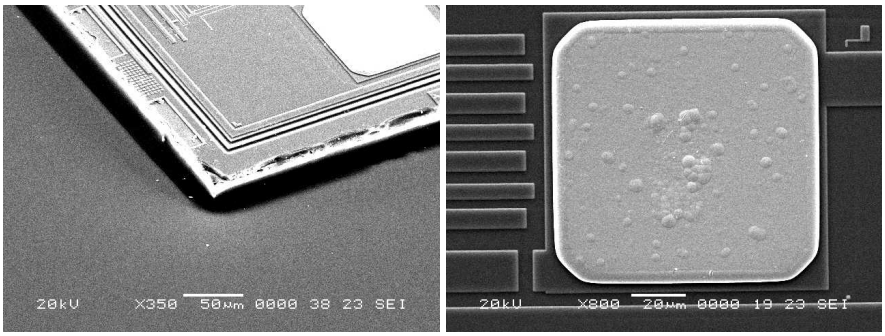


(a)



(b)

Figure 4.16: Flatness of the $20\mu m$ thick EEPROM Chip analyzed by Wyko profilometer (a) After placement by Tresky on the spin coated BCB, (b) After full curing of BCB.



(a) (b)

Figure 4.17: SEM analysis of the $20\mu m$ thick EEPROM Chip bonded on the PI film (a) Tilted image showing chip thinness and BCB spreading out of the chip edge, (b) Clean contact pad (Ni/Au-bumped) of chip after the complete chip bonding process.

4.4 2nd and 3rd PDPI layer

Once the chips are placed flat and well-aligned with respect to the alignment structure on the carrier, it is easy to make flattening layer. The basic technology for making this layer is developed by the UTCP group in CMST [69]. This can be implemented in the case of samples carrying multiple chips as each chip acts like a mask for the photo lithographic development (Figure 4.6, step4) of the PDPI layer creating self-aligned cavity.

Via processing on the contact pads needs fine alignment. If the chips are bonded on the substrate with high accuracy, it is possible to develop photo-via on all the chips by global alignment followed by single photo lithography step. To demonstrate this via processing capability, 4 PTCE test chips of size $5 \times 5mm^2$ precisely placed with a separation of $34mm$ on a substrate. They were assembled by using the same PDPI HD4110 as adhesive glue at HighTec [34] during TIPS project. The substrate used in this case is a 4" square white float glass carrier with $20\mu m$ thick PDPI HD4110 spin cured on it. Each of these PTCE chips contains daisy chain pattern with 44 contact pads of size $100 \times 100\mu m^2$ and pitch $200\mu m$. After making the flattening layer, photo-vias of dimension $50 \times 50\mu m^2$ were opened on the contact pads (176, in total). Figure 4.18 illustrates photo-vias opened on all the chips by a single lithography step. As the chip bonding process on the base PDPI surface was not optimum (bad adhesion and voids under the chip), the samples could not be used for further fabrication process.

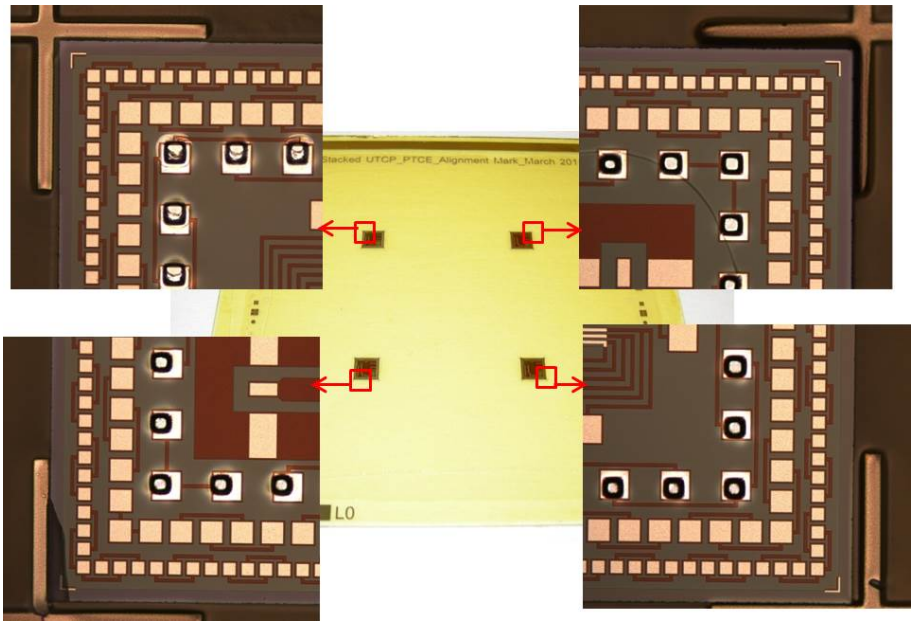


Figure 4.18: Photo-vias opened on 4 PTCE test chips each containing 44 contact pads by single photolithography step

4.5 Conclusion

The Flat-UTCP technology and the related issues for stacking application are discussed in this chapter. CTE of different materials plays a role in making the whole package symmetric and this in turn affects the level of package deformation. This has been illustrated in details by calculation and experimental results. Another way to control the deformation level can be introduction of stress relief patterns in the polyimide layers. However, this has not been verified experimentally by measuring the shape and the size of the patterns after processing. This strategy is first implented in the demonstrator fabrication which is going to be discussed in chapter 5.

Thin chip assembly with complete bonding on the PI is a yield limiting factor in the fabrication process. Voidfree placement of flat chips with an alignment accuracy of $\pm 10 \mu m$ has been achieved by using different intermediate layers between the chip and pick-up tool. The adhesive glue (BCB) curing process is the most critical process which needs more attention in order to avoid overflowing of the BCB on the chip surface.

Considering all these factors, the process flow for producing multiple Flat-UTCP has been modified and will be discussed in Chapter 5.

Chapter 5

Stacking of Photo definable Polyimide based Flat-UTCPs

5.1 Introduction

In the previous chapter(s), the process for 3D-stacking of Ultra-thin chip packages (UTCP) is discussed which provide an effective way for fabricating devices with a minimal package volume. An overview of this technology resulting in the fabrication of a $300\mu m$ thick stack of 4 EEPROM memory dies has been presented in chapter 3. This process is based on the first generation of UTCPs which consists of a chip embedding technology within two spin-on polyimide layers [18]. The polyimide membrane of these packages has a total thickness of $40\mu m$, however where the thinned die is embedded a topographical difference of $15\mu m$ to $35\mu m$ exists. Furthermore, the presence of the silicon die results in more or less flexible areas in the interposer. The combination of both mechanical characteristics resulted in an increased risk of die cracking during the lamination process. This effect has been reported in chapter 3. In order to control this risk of cracking, the topography can be reduced, thus creating a "Flat-UTCP" (Figure 4.1).

According to the stacking concept described in chapter 3, the presence of one non-functional package in the stack makes the whole stack non-functional. To reduce the stacking yield loss due to this effect, a symmetry in package distribution is introduced. In this paper, the development of such Flat-UTCPs with a high stacking yield is discussed.

5.2 Overview: 3D-Stacking of Ultra-Thin Chip Package Process

The whole process can be divided into two parts.

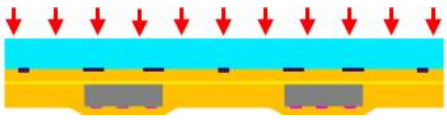
- UTCP fabrication process
- UTCP stacking process

5.2.1 UTCP fabrication process

More details about this whole technology is given in chapter 4. Considering the CTE mismatch and precise chip placement issues, the multiple Flat-UTCP process is modified and shown schematically in Figure 5.1.

(a) Step1. Spinning and curing of PDPI 4110 on glass carrier with alignment mark and release layer

(b) Step2. Precise placement and bonding of multiple chips



(c) Step3. Spinning of flattening PDPI layer and backside illumination through the transparent carrier

(d) Step4. Self-Aligned cavity for chips and stress-relief grooves on PI after the PDPI development

(e) Step5. Micro-via opening on covering PDPI by Photolithography

(f) Step6. Metal deposition and patterning

Figure 5.1: Process flow for multiple islands of Flat-UTCPs on a single carrier

In this process, 2" square glass with a thickness of $0.7mm$ is used as carrier. For precise placement of chips, a $50nm$ thick TiW alignment layer is sputter deposited and patterned on the glass carrier. It is then followed by a selective deposition of salt (KCl) layer for easy release of packages after fabrication. The first polyimide layer (PDPI HD4110) is spin-cured on the carrier and acts as a base PI layer for the UTCP process. After bonding the thin-chips on the base PI layer, second PI layer which is the flattening layer, is processed with introduction of stress-relief grooves in the whole package. These grooves divide the large area of multiple chip-packages into pseudo-small islands of packages, each carrying one single chip per package. Photo-via on the contact pads of the chips are opened on the third or covering PDPI layer of the package. Contact to the external world is made by a fan-out metallization on the package which is achieved by deposition and patterning of an $8\mu m$ thick copper layer.

5.2.2 UTCP stacking process

An ideal fabrication process should have the capability to give 100% production yield. However in mass production of the UTCP packages, the yield will be lower. The yield (η) of the process flow for individual UTCP packages has been verified to be higher than 85%, based on the measurement of the functionality of several commercially available off-the-shelf ICs (MSP430F1611, nRf24L01, in-house ASIC design, etc) [67]. When n UTCP-packages are stacked, one single non-functional UTCP will result in a non-functional stack. Therefore the stack yield (η_u) will drop to $\eta_u = \eta^n$. In case of 4 stacked EEPROM dies, the maximum yield will be 0.85^4, or 52%. The effective yield (η_{eff}) of the whole stacking process will be lower as the above mentioned value needs to be multiplied with the yield η_s of the stacking process itself.

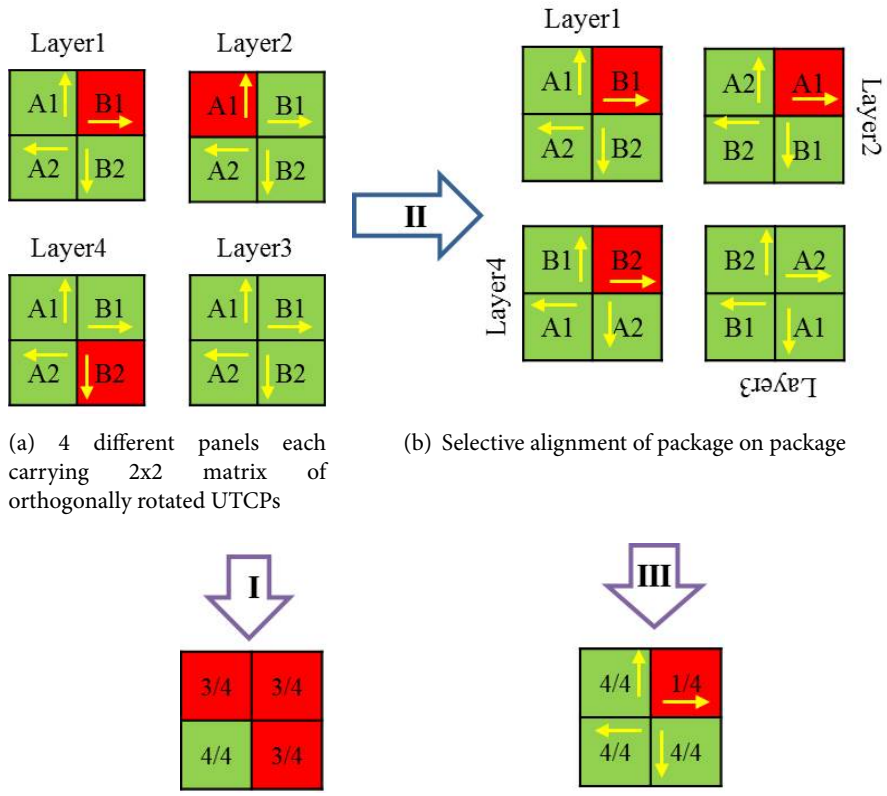
$$\eta_{eff} = \eta_u \times \eta_s \tag{5.1}$$

The stacking yield of the non-flat two-layered UTCP has been found to be $\eta_s \approx 15\%$. This has been verified by doing a back calculation (in section 3.5) which results in an overall yield η_{eff} of 7% following the simple equation on yield calculation (Equation 5.1). As discussed in section 3.5.1, topographical difference in the package (higher package thickness at the chip positions) adds the risk of die cracking during stacking process and this results in a very low η_s value for the conventional 2-PI layered UTCP technology. By adding a third polyimide layer, thus introducing the Flat-UTCP concept, this risk during the lamination process can be reduced and as a consequence the η_s value will increased.

PoP Alignment

The above mentioned calculation is based on the process where individual package positions per panel are fixed per substrate. With this type of package distribution, there is no freedom to eliminated the non-functional packages before stacking. However after release of each individual UTCP layer or sheet the functionality of the individual UTCP packages can be checked, and the known-good-packages are allocated. Introduction of a new symmetry in package distribution per substrate makes the elimination process easy before lamination. With this symmetry, packages can be selectively aligned on each other after knowing the position of faulty ones. Considering a large scale production process, η_u value can be modified by introduction of this symmetric factor.

On a flat rigid carrier, these multi-UTCP packages can be fabricated with a symmetry in their position. As discussed in section 3.5, packages per panel are arranged in a matrix form with translational symmetry. To eliminate one package, the whole row or column of packages has to be wasted by shifting the position via translation. In the similar situation, a rotational symmetry in the distribution can easily eliminate the non-functional one by selecting the appropriate angle of rotation. As a result, this rotational symmetry in multi-chip packages helps in improving yield in 3D stacking process.



(a) 4 different panels each carrying 2x2 matrix of orthogonally rotated UTCPs

(b) Selective alignment of package on package

(c) Yield per panel by two different approachs

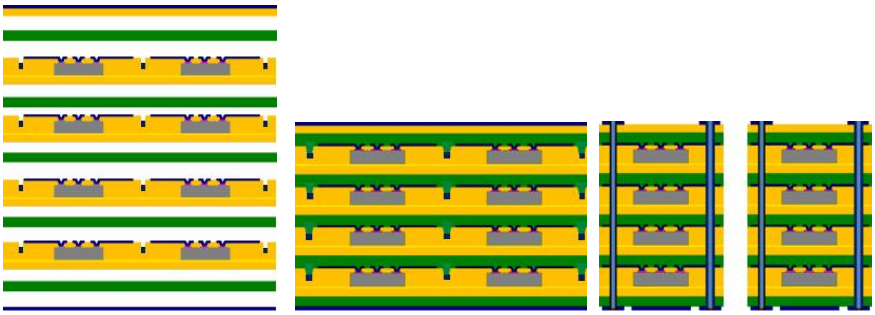
Figure 5.2: Difference in the two stacking approaches: I. without selective alignment of packages giving rise to 3 non-functional stack of 4, II. With selective alignment by rotation and stacking (III) afterwards gives 1 non-functional stack out of 4.

For stacking packages with different type and dimension of dies, it is more convenient to fabricate them separately on different carriers which was done in the previous case (chapter 3). Additionally, order of the packages in the stack is an important factor in some critical applications (e.g, inclusion of RF chip package). However, the same concept of rotational principle can be applied in the package orientation. After release from the carrier, a single panel will contain multiple packages with rotational symmetry. By knowing the position of the non-functional ones per panel and number of such positions per batch, they can be easily eliminated from the stack by choosing the proper angle of rotation during package-on-package alignment.

For stacking of 4 packages, they can be fabricated on 4 different carriers where each carrier will contain same packages (chip, and/or metal layout). As demonstrated in Figure 5.2, four such panels contain orthogonally rotated packages in a 2×2 matrix

form. Each of them has distributed non-functional packages. Taking the advantage of rotational symmetry, different UTCP sheets are rotated in such a way that the non-functional UTCP's are aligned on top of each other. This results in increasing the number of functional stacks from 1 (stacking in conventional way) to 3 (stacking after selective alignment via rotation).

Following the alignment principle shown in Figure 5.2, four of these sheets with two additional flexes on top and bottom are stacked together by vacuum lamination technology (as described in chapter 3). Upilex foil SR 1410 from UBE Inc. of $25\mu m$ Polyimide/ $9\mu m$ Copper and Cu Flex (TW-YE) from Circuit foil of Cu thickness 9µm are used as top and bottom layer, respectively. For package-on-package bonding, $25\mu m$ thick adhesive films Pyralux LF 100 (from Dupont) is used in between each of these layers during lamination process. The interconnection to each of the embedded packages is made by laser drilling of through hole vias on the external contact pads. This is followed by metallizing the through holes by electroless-galvanic Cu deposition and patterning them using lithography. This results in the production of $\sim 360\mu m$ thick stacked module with 4 dies embedded inside. The schematic overview of the process flow is illustrated in Figure 5.3.



(a) Aligning 4 layers of multiple UTCPs, LF100 as bonding material in between each two layers, Cu flexes on top and bottom, prior to stacking

(b) Stacking of all layers by vacuum lamination

(c) Singulated stacks after making through hole via interconnection by Laser drilling, followed by plating, patterning and dicing

Figure 5.3: Schematic overview of stacking of Flat-UTCPs process flow

5.3 Design and Fabrication Process

This new concept of stacking is demonstrated in lab scale fabrication process by stacking of 4 EEPROM memory die packages. The circuit design of this stacked module is provided by Oticon [60] for the specific purpose of mounting it in a Hearing Aid Device (ref. chapter 3). As per this stack design, package order within the stack is not a factor to be considered. This means packages with four different sets of lay-outs

can be in any order within the stack. Combining this with rotation principle during package-on-package alignment, the mask making cost can be reduced by making 4 different layouts on the same mask.

The EEPROM chips are aligned and bonded on the PI substrate in a 2×2 matrix form having a $90°$ rotational symmetry as shown in Figure 5.6-a. As a result, this gives rise to 4 EEPROM packages with different metal layouts on the same carrier. After release from the carrier, four of such panels each containing 4 different layouts can be selectively aligned by rotation. This rotation has to be made in such a way that each of the stack will contain 4 packages of different layouts.

5.3.1 Substrate Preparation

First step of UTCP production process is cleaning of the 2" square glass carriers by conventional process. This includes overnight soaking in RBS soap solution, rinsing by isopropanol and deionized water. To align thin-dies on the substrate, a metal pattern is processed by sputter deposition of $50nm$ thick TiW on the whole surface, followed by patterning it by the mask design described in Figure 5.4.

Together with the alignment marks (Figure 5.4-b) for precise placement of chips, some extra lines and alignment structures (Figure 5.4-c) are designed on the same mask. A rotational symmetry in the chip alignment mark can be visualized within the 2×2 matrix made by equi-distance lines of width $100\mu m$. These lines are designed to transfer it to flattening polyimide layer to create stress-relief pattern. The alignment marks (Figure 5.4-c) are used in the next alignment step for making photo-vias on the contact pads of precisely placed chips.

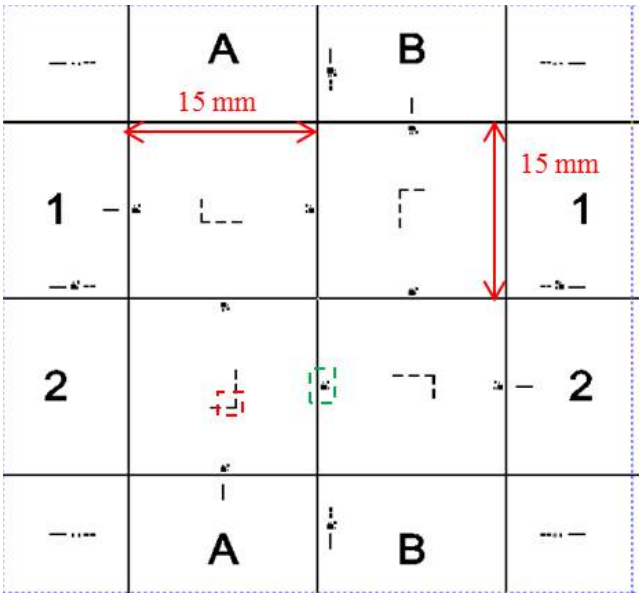
As per the general UTCP process flow, KCl (release layer) is selectively deposited on the substrate by thermal evaporation method. The edges of the carriers are protected from salt by wrapping Aluminum foils which covers $4mm$ from each side. This prevents direct adhesion of base layer on the glass edge due to the self-priming property of the PDPI HD4110.

5.3.2 Base PDPI (1st) layer

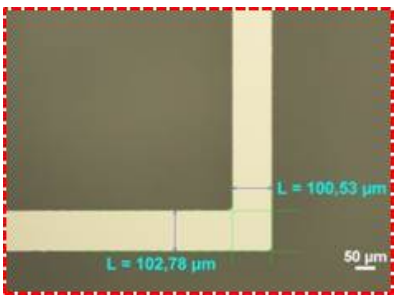
To get a cured polyimide film of thickness $\sim 18\mu m$ as a base layer of UTCP on the carrier, the photo definable polyimide (PDPI) HD4110 is spin coated and fully cured with the following set of parameters.

- Spinning polyimide for $10s$ at the speed $1000rpm$ for spreading all over the carrier surface, followed by $1min$ at the speed $1800rpm$ for thinning down to required thickness. Pre-baking on hot plate for $4min$ at $115°C$. Minimum $5min$ cooling time.
- UV exposure for $38s$ with light intensity $4.9mW/cm^2$
- Full curing of polyimide film inside vacuum chamber in N_2 environment with a flow rate of $5sccm$. The curing cycle includes temperature ramping from

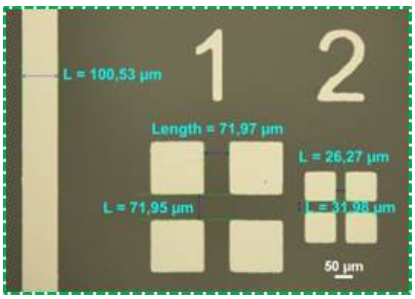
room temperature to $200°C$ with a ramp rate of $4°C/min$, holding at $200°C$ for $30min$, 2nd ramping step up to $375°C$ with a ramp rate of $2.5°C/min$, full curing at that temperature for $1h$ and cooling down to room temperature.



(a) Design for chip alignment and stress relief pattern on PI



(b) Chip alignment pattern defined on the carrier by TiW patterning



(c) More alignment + stress relief pattern for PI processing

Figure 5.4: (a) Design made for precise placement of 4 chips on 1st PI layer, stress-relief grooves on 2nd PI layer, alignment patterns for photo-via definition on 3rd PI layer, (b) Chip alignment pattern defined on the carrier by TiW patterning, (c) Pattern on carrier for stress-relief groove on flattening layer of UTCP (left), alignment marks during photo-via definition on the contact pads of multiple chips by photolithography step(right)

Before applying the next thin film on the fully cured base polyimide layer, the PDPI surface preparation(roughening) is a necessary step for a better adhesion. In this process, a plasma treatment by reactive ion etching (RIE) of the PI surface is done with the following process parameters inside the RIE chamber maintained at power $150W$ and pressure $100mTorr$.

- $2min$ in CHF_3/O_2 gas environment with a flow rate of $5/20sccm$ respectively.
- $2min$ in O_2 gas environment with a flow rate of $25sccm$

5.3.3 Multiple Thin-Chip placement

As per the process development discussed in Section 4.3.4, the thin chips are placed and bonded on the PDPI layer using BCB (cyclotene 3022-46) as glue. This BCB is spin-coated on the PDPI surface for getting a uniform thickness. The spinning speed was $500rpm$ for $10s$ for uniform spreading, followed by $3000rpm$ for $30s$ for thinning down to $\sim 3\mu m$. To evaporate some of the solvent content, BCB is pre-baked on the hot plate at $100^{\circ}C$ for 1 min in clean room atmosphere.

The thin chip is picked face-up by a vacuum tool of Dr. Tresky's fine placer and aligned optically by matching the back side edge of the chip with the alignment mark patterned on the carrier (Figure. 5.4-b). Although this pattern was covered by the $18\mu m$ thick PDPI and $2\mu m$ thick BCB, the visibility was good enough for this alignment. The applied force during placement is $300g$ on a $20\mu m$ thick EEPROM die of size $2 \times 3.5mm^2$ for the duration of $2min$ at $150^{\circ}C$. At this temperature, the underlying pre-baked BCB starts liquefying which is a requirement for pre-bonding of the chip on the substrate. After this process and before placing the next chip on the same substrate, the locally heated chip together with BCB on the carrier was allowed to cool down at least for $10min$ to avoid thin die shifting. The spacing between chips was maintained at $15mm$ to eliminate a radial deformation in thickness of BCB which has been noticed due to local heating during chip placement process. If the chips are placed closely enough, the flatness after placement cannot be maintained due to non-uniformity in BCB thickness. After placing 4 chips with a rotational orientation on a single substrate, the BCB is fully cured in 3 steps.

BCB Pre-curing:

This process consists of temperature ramping up to $150^{\circ}C$ with an average heating rate of $4^{\circ}C/min$, $30min$ holding at $150^{\circ}C$, cooling down to room temperature. At this stage, BCB starts flowing. There is a chance of chip movement and getting voids under the chip during this phase. This can be controlled by applying a pressure of $1bar/die$ on the top of the chip from the beginning till the hot plate cools down to room temperature.

For pressure uniformity, the 4 chips on the carrier is covered by a glass carrier with a $20\mu m$ thick Teflon layer as an intermediate layer. A load equivalent to the pressure for 4 dies is applied on top of the covering glass. Teflon layer prevents the BCB at the bonding

area to come in direct contact with the covering materials. With this combination, a minor shift of thin die has been noticed several times. The reason is thinness of the Teflon sheet and porosity in it, which allows BCB overflow on the entire chip surface. Although a load is applied from top, the movement of this layer together with chip cannot be completely avoided. Therefore, the Teflon sheet is attached to the covering glass by a thermal release tape which can hold it during the complete temperature cycle. The whole stack is well aligned and placed on the hot plate as shown in Figure 5.5 before starting the curing process.

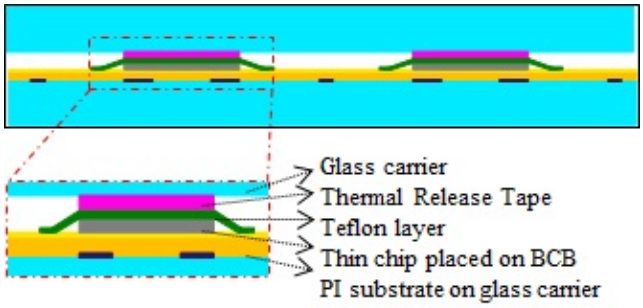


Figure 5.5: Schematic cross-sectional view of the stack build up with temporary carrier and release layers over the chip during the bonding process

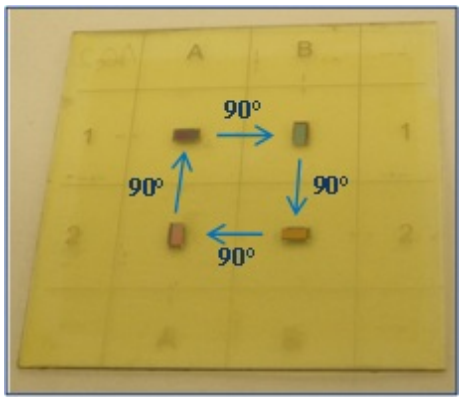
BCB Half-curing:

With the same heating profile, the BCB was half-cured at $210°C$ for $30min$ with a pressure of $1.7bar/die$. At the end of this process, the BCB changes to semi-solid phase.

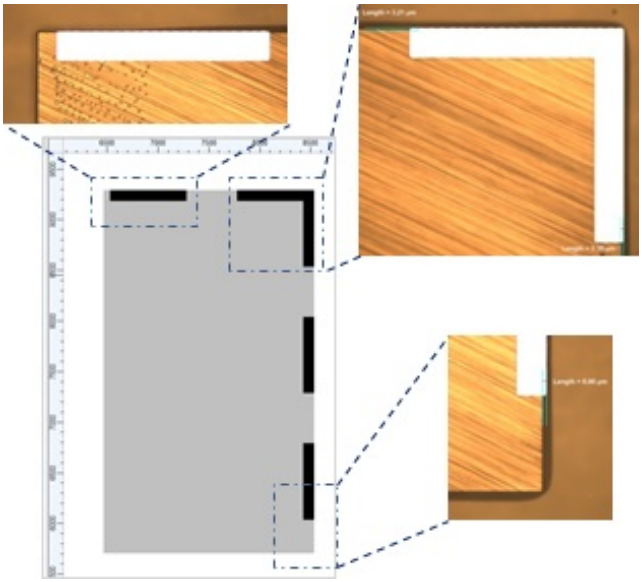
BCB Full-curing:

For final bonding of chips onto the PDPI substrate a pressure of $2bar/die$ is applied on the top and BCB is cured at $260°C$ for $1h$. This full-curing process is performed in a conventional oven with N_2 ambient.

Figure 5.6 shows the final result of the chip placement and bonding experiments implemented in producing 4 well-aligned chips on a single substrate. The reproducibility of the process has been verified by repeating this process in fabrication of 14 of such samples for multi-UTCP fabrication process. As a standard technology, the same surface roughening treatment is repeated before applying next layer for a good adhesion.



(a) Orthogonally rotated 4 chips placed precisely on semi-transparent PDPI HD4110 base layer



(b) Back side view of chip edge with respect to the TiW-alignment mark

Figure 5.6: (a) Orthogonally rotated 4 chips placed precisely on semi-transparent PDPI HD4110 base layer looking through the alignment pattern on the 2 " glass carrier. (b) Back side view of chip edge with respect to the TiW-alignment mark in the design file and the corresponding view through the glass carrier; placement accuracy of $\sim 10\mu m$ is achieved.

5.3.4 Flattening PDPI (2nd) layer

The chip thickness together with underlying BCB is measured, to determine the PDPI thickness required for making the flattening layer. The corresponding spinning speed is determined from the spin curve [40]. The maximum thickness which can be achieved by spinning and curing this PDPI is $20\mu m$. Multiple spinning steps are required to cover the chip with thickness more than $25\mu m$ for complete planarization. In this particular case, the chip + BCB thickness was measured to be in the range of $21-22\mu m$. A single PDPI spinning step was enough to make the flattening layer. A mismatch of $1 - 2\mu m$ can be planarized during the final PDPI layer processing. The following sequence of processing steps is executed for this flattening layer processing. These are the standardized set of parameters used at CMST for flattening layer processing.

- Spinning PDPI HD4110 for $10s$ at $1000rpm$ for uniform spreading, followed by $1min$ at $1500rpm$. Pre-baking on hot plate for $4min$ at $115°C$. Minimum $5min$ cooling time.

- Taking the advantage of negative photo sensitivity, backside illumination of UV enables PDPI patterning for self-aligned cavity for chips. In this case, the Si-chip attached to the carrier acts as a mask when the assembly is UV exposed from the back of the carrier (step3, Figure 5.1). In addition to that, the equidistant lines with a width of $100\mu m$, present on the carrier (Figure 5.4-c) are patterned on the same layer of polyimide in the same process. The UV exposure time was optimized as $2min$ with a light intensity of $10mW/cm^2$ for this backside illumination process. The light has to pass through the transparent glass carrier of thickness $0.7mm$ and a semitransparent fully cured thin film of base PDPI layer. After exposure, minimum $10min$ holding time before development to stabilize the polymerization process is required.

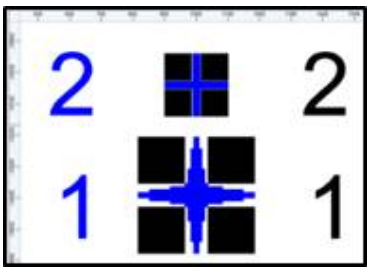
- PDPI development in dedicated developer PA-400D and PA-400R from HD Microsystems. In this process, the sample is immersed in a beaker containing PA-400D for $1min$ with ultrasonic agitation, followed by $30s$ in a $1:1$ solution of PA-400D and PA-400R, $30s$ rinsing in PA-400R, finally drying by N_2 blow-off. Post development waiting time minimum $10min$.

- Full curing of polyimide film inside vacuum chamber with same set of parameters as for base PDPI layer.

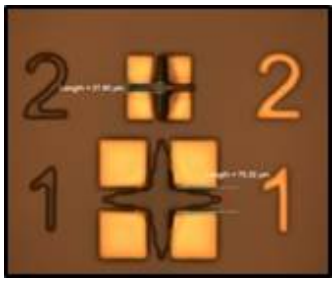
- PDPI surface roughening by the above said standardized RIE process.

5.3.5 Covering PDPI (3rd) layer

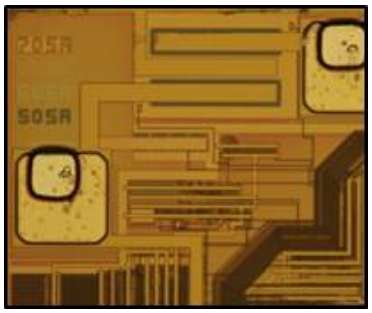
The EEPROM die contains 8 contact pads of size $103 \times 103\mu m^2$ with $90 \times 90\mu m^2$ pad opening, out of which 7 are used for making interconnection in the 3D-stack of packages (ref. to Chapter 3, Figure 3.1). The micro-vias of size $50 \times 50\mu m^2$ are opened on the contact pads of the 4 chips by a single lithography step.



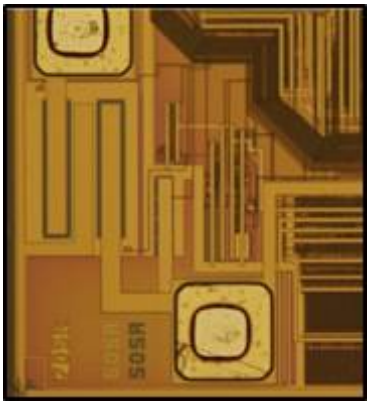
(a) Alignment mark on via mask (blue), on carrier (black)



(b) Alignment mark defined on PDPI after via processing



(c) Via position shifting



(d) Centralized via on contact pad

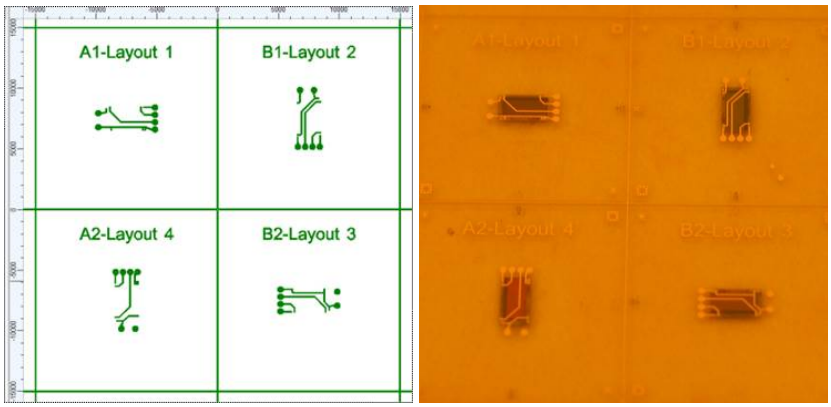
Figure 5.7: Alignment mark (a) designs on the via mask (blue) and on the carrier (black), (b) Defined on the PDPI layer after via processing, (c) and (d) Micro-via of size $50 \times 50 \mu m^2$ opened on the $90 \times 90 \mu m^2$ size contact pads of the multiple chips the placed on the same substrate. Shifting of via position from the center of contact pad is a consequence of chip misalignment.

The cover PDPI layer is spin-coated and developed with the following set of parameters to get a final thickness of $15 \mu m$ after curing.

- Spinning PDPI HD4110 for $10s$ at the speed $1000rpm$ for uniform spreading, followed by $1min$ at $2000rpm$. Pre-baking on hot plate for $4min$ at $115^{\circ}C$. Minimum $5min$ cooling time.
- UV exposure for $38s$ with light intensity $4.9mW/cm^2$ after alignment of the sample under the via mask. The alignment marks used for this process are illustrated in Figure 5.7. Minimum $10min$ holding time after exposure.
- Same development, full curing and after curing surface roughening step as for previous PDPI layer.

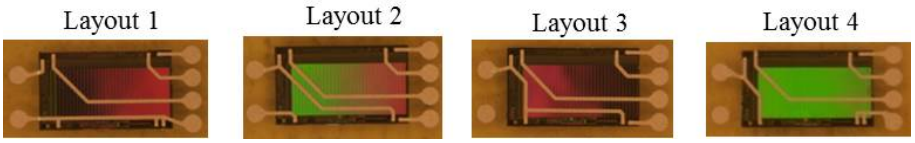
5.3.6 Metallization and Patterning

Each sample now contains 4 embedded thin dies with micro-vias open on the Ni/Au finished contact pads. For making the metal fan-out from the contact pad of the chip to the external surface, the first step is a seed layer deposition on the entire sample. This is done by loading all the samples together in a sputtering machine for sputter deposition of TiW($50nm$) + Cu($1\mu m$). In the next step, the copper is thickened up to $8\mu m$ by a conventional panel plating process. The metal is finally patterned by using a standard lithography and wet chemical etching process. The mask used for the metal patterning contains four metal layouts with orthogonal symmetry as per the chip orientation on the carrier (Figure 5.8).



(a) Four layouts on the same mask

(b) Four UTCPs with different metal layout on the same carrier



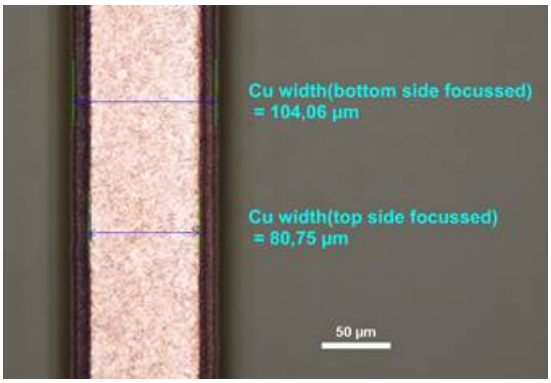
(c) Close view on the pattern definition

Figure 5.8: Four different metal layouts (L1-L4) on the same mask with orthogonal orientation to facilitate high yield during stacking process.

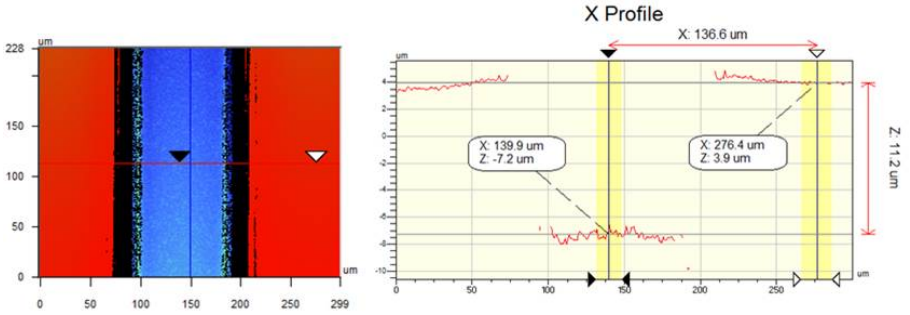
5.3.7 Stress-relief pattern

The spacing between the center of each Flat-UTCP and the stress-relief groove is maintained at $7.5mm$. The mask used for metal patterning on UTCPs contains the lines of $100\mu m$ width which protects the copper deposited inside the grooves. After metal patterning, the profile of this stress-relief groove is studies by optical microscope and wyko profilometer (Figure 5.9).

The copper width varies from $80\mu m$ (top) to $100\mu m$ (bottom) in this groove. The polyimide profile and copper profile are created by two different ways of UV exposure and photolithography. The 1st one is by backside illumination and 2nd one by front side UV exposure. The step height at this region after the 1st lithography step is same as the flattening layer thickness, $20\mu m$. After metal patterning, the cavity gets filled with copper up to $8\mu m$. This finally gives a step of height $10 - 12\mu m$ from copper (bottom) to the polyimide (top).



(a) Copper track width within the PI groove



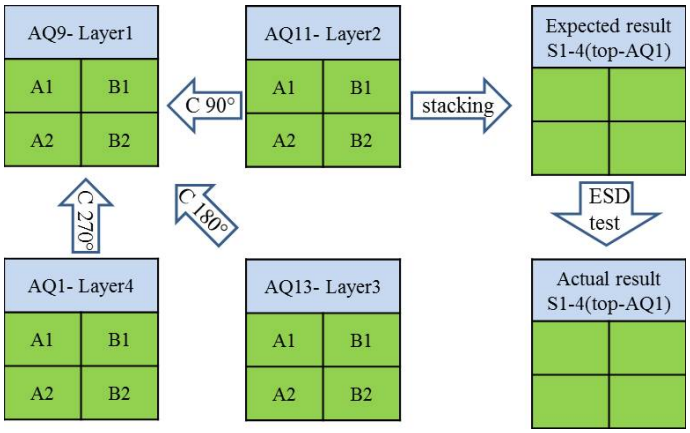
(b) Step height at the PI groove filled with copper

Figure 5.9: Top side view of the stress-relief pattern (a) copper track width measurement by optical microscope, (b) step height measurement by wyko surface profilometer.

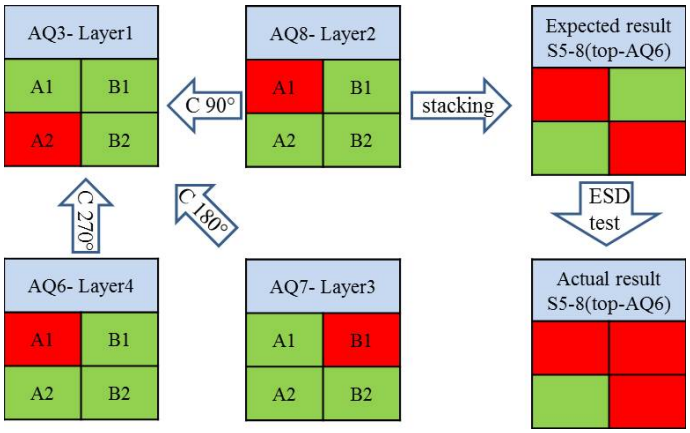
5.3.8 Functional package mapping

The ESD pads on the chips are tested after the UTCP fabrication process to map the good ones per sample before going to the stacking process. Eight separate substrates each carrying four UTCPs have a random yield which is 75% in 3 panels (3 functional out of 4) and 100% in the rest of the 5 substrates (Figure 5.10). This in average gives

a UTCP yield (η) of 90%. With the mapping of functional ones and taking advantage of rotational symmetry in the package distribution, the layer by layer rotation of the released UTCP panel can be easily set to get maximum number of working stacks.



(a)



(b)

Figure 5.10: Functional package/stack mapping on each panel before and after stacking showing yield per panel(green: functional, red: non-functional)

5.3.9 Deformation after UTCP release

The copper alignment mark positions at the extreme corners of the UTCP panels are checked before its release from the rigid carrier. This helps in keeping track of deformations in the package and the stack after completing the fabrication process. The PDPI has a good adhesion at the edge of the carrier. For the release of this package, a cutting is made on the polyimide layer covering the release layer. YAG laser is used

for the precise release of the package. The back side of the package facing the salt can be rinsed afterwards by DI water.

The shift in alignment mark position (inward) after release from the carrier is the sign of deformation in package. This value remains the same even after laminating them to stacked packages. In the current process, where stress-relief grooves are introduced in the polyimide film, a linear shrinkage of 0.3% has been observed. This is comparatively less as compared to 0.9% which was found in larger sample of size $8 \times 8cm^2$ fabricated on a 4 " square glass substrate (Section 4.3.2). To apply this method in an industrial level fabrication process more investigation should be done on incorporating this stress-relief patterns in large area package production process.

5.3.10 Lamination and Interconnection process

After release, the UTCP stacks are fabricated as per the alignment concept and following the process flow shown in Figure 5.2 and Figure 5.3, respectively. The layer by layer flexes are laminated temporarily on hot plate after optically aligning them (Figure 5.3, step1). The step by step process for alignment is given below.

- All the UTCP flexes are baked on a hotplate for $2min$ at $120°C$.
- Roll Lamination of $25\mu m$ thick LF 100 adhesive glue onto $9\mu m$ thick Cu sheet (bottom layer of stack) on a hot plate at $90°C$ for $10s$.
- Placing the 1st layer of multi-UTCP on the adhesive layer and next LF 100 layer and laminating them together at $90°C$ for $10s$ on the hot plate.
- Aligning next UTCP layer with respect to previous layer with necessary angle of rotation which helps in reduction of the non-functional stack count.
- Temporarily fixing the position of the packages by local heating of the adhesive at certain points.
- Repeating the adhesive glue lamination and UTCP sheet alignment by rotation process up to the final covering layer Upilex foil of $25\mu m$ Polyimide + $9\mu m$ Copper.

The whole stack is then laminated by vacuum lamination technology as discussed in chapter 3. The through hole via (THV) drilling at the stacked contact pads is done by YAG Laser. The through holes are plated by electroless and galvanic copper deposition. The top and bottom side Copper patterning is made by dry film resist based lithography and a wet chemical etching process. This THV technology for making interconnections is discussed in detail in chapter 3. The fully fabricated stacked EEPROM UTCPs is shown in Figure 5.11. The complete laminate contains 4 stacks in 2×2 matrix form and each stack with having 4 Flat-UTCPs.

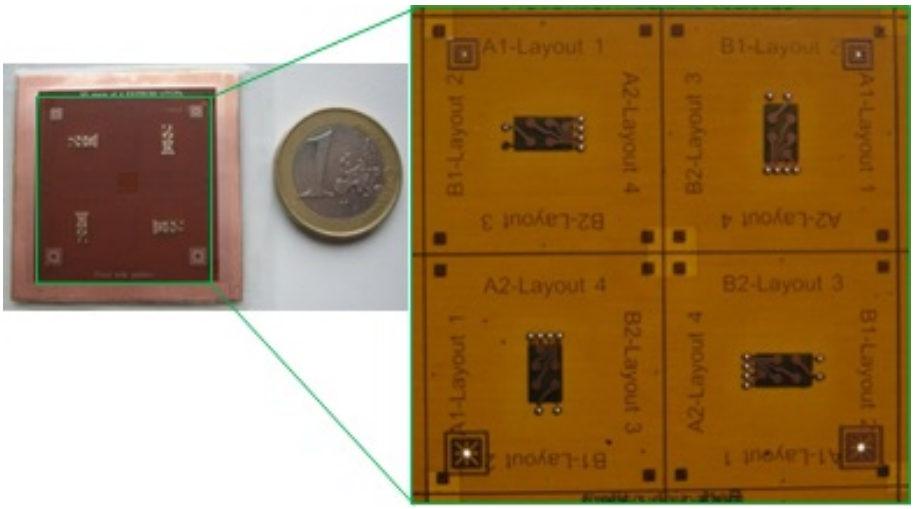


Figure 5.11: Front side view of 2x2 matrix of 4 stacks of EEPROM UTCPs (16 Flat-UTCPs in total)

5.4 Result and Yield Analysis

The difference in two versions of stack (as shown in Schematics diagram, Figure 4.1) can be visualized from the X-ray CT scan pictures (Figure 5.12). This analysis gives a clear picture of the metal profile within the stack. A close-up view on the copper routing from the contact pad of the chip to the plated through hole is shown in Figure 5.12-b,c. The copper patterned on the packages follows the topography of the underlying layer. This can be verified for the two cases by wavy copper routing at the non-flat chip edge (Figure 5.12-b) and straight ones in case of flat chip edge (Figure 5.12-c). The micro-via pattern on the contact pads of the chip are different in both the cases. In the first case, the via is defined on the non-photodefinable PI surface by use of YAG laser [18]. The via size dependes on the beam shaping optics of the laser which is smaller and less reproducible as compared to that in case of photo-vias defined on PDPI. The copper track from the photo-via on the contact pad to the chip edge of the flat package (dotted region in Figure 5.12-c) is shown in the cross-section picture (Figure 5.12-d).

The cross-section of stacked package (Figure 5.13) shows the chip edge region of the 3D-stacked Flat-UTCPs. The 3-layered polyimide packages of thickness $\sim 50\mu m$ result in an entirely flat package at the chip edge due to inclusion of an extra flattening layer. As a result, this makes the whole stack flat with a total thickness of $360\mu m$.

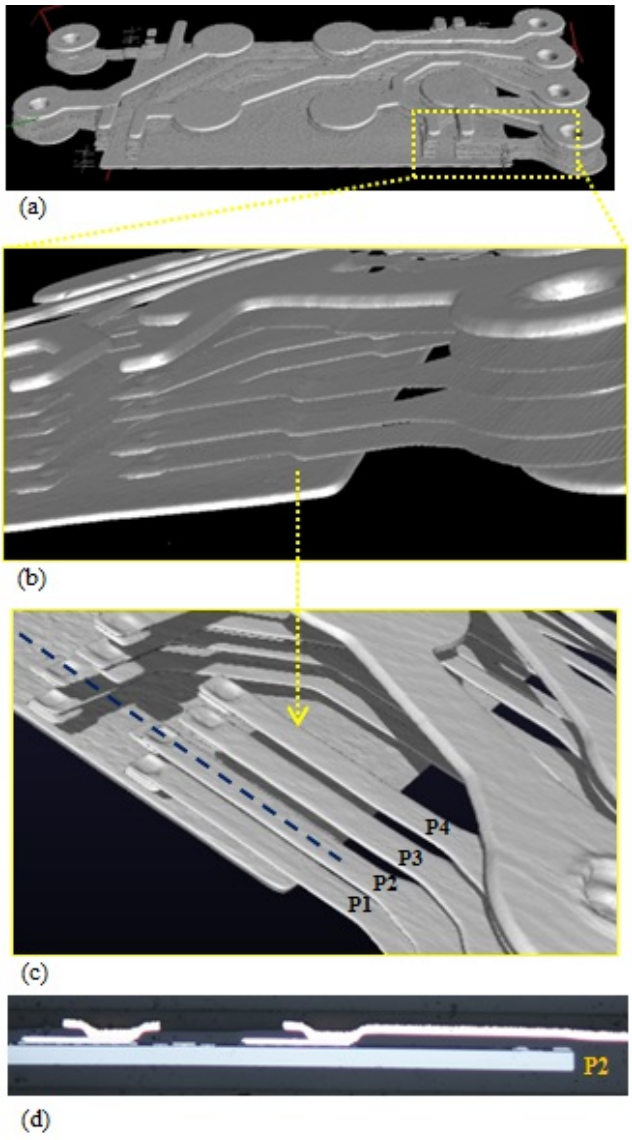


Figure 5.12: (a) X-ray CT scan picture of one stacked UTCP showing only conductive lines within the stack, (b, c) close-up view at the Cu routing from the chip contact pads to the TH pads of stack of conventional UTCPs (non-flat) and Stack of Flat-UTCPs, respectively, (d) cross-section view of one the package within the stack at the region marked in (c).

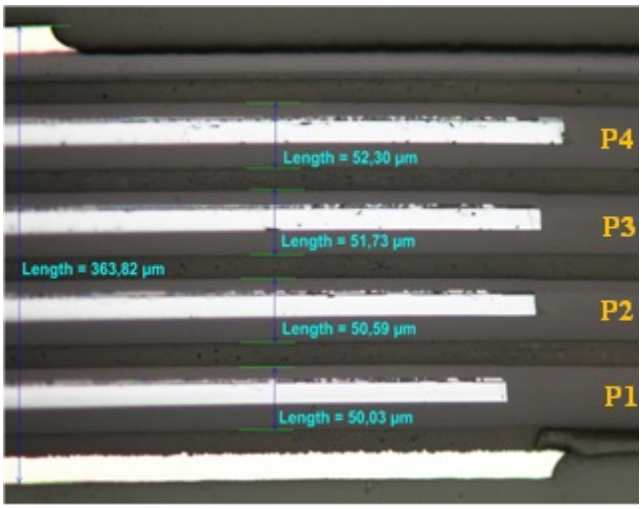


Figure 5.13: Cross-sectional view of stacked Flat-UTCPs showing uniform package thickness at the chip edge

In the whole process, chip placement is the most critical step which brings down the average yield (η) of the current UTCP process to 90%. The yield figure η_s, following previous PoP alignment principle can be estimated as 0.9^4 or 0.65. Following the rotational symmetry in PoP alignment, the η_u value can be calculated as 87.5% (7 working stacks out of 8). The ratio of these two values can be denoted as rotational symmetric factor (η_r) in the package. For stacking of higher number (n) of packages, this symmetric factor (η_r) can improve the overall yield (η_u) by applying rotation law. In that case, the packages have to be arranged in a circular pattern on a round carrier which makes the rotation easier. Depending on the package size, deformation limit and mass production facility, the size of the carrier can be selected. Additionally, the use of a circular carrier will help in achieving thickness uniformity in the spin-on layers used in package fabrication.

In the current process, the order of packages in the stack was not considered. Therefore the different metal layouts are designed on the same mask and transferred onto the packages. This results in producing UTCPs of different metal layout on the same panel. However this approach adds another risk to the rotation law when a number of packages with same metal layout on different panels becomes non-functional. Although theoretical calculation gives 7 working stacks out of 8, this number drops down to 6 due to this above said risk. To apply this approach in production process, it is recommended to fabricate packages of the same type on a single carrier.

From all the above said calculations, the estimated η_u value was 75% (6 working stacks out of 8). ESD pad test resulted in 5 working out of 8 stacks which gives $\eta_{eff} = 62.5\%$. From equation 5.1, the stacking yield (η_s) can be calculated as 83% which shows a

significantly high impact of the Flat-UTCP in the whole process as compared to 15% in case of conventional UTCP stack.

5.5 Conclusion

An improved technology to produce 3D-stacks of ultra-thin chip packages with higher yield has been reported in this chapter. The most important factors that affect the overall yield in this UTCP stacking process are flatness at the chip edge of the package and symmetry in the package distribution.

The Flat-UTCP fabrication process includes the risk of thin chip handling and polyimide deformation due to CTE mismatch. To make this process faster and more accurate, different placement process needs to be developed. More investigation can be made for deformation control in the package by using different stress-relief patterns which in turn facilitate the large area production of Flat-UTCPs using PDPI.

Rotational symmetry in package distribution has a role in improving stacking yield. The exact quantitative figure cannot be generalized for the current process as the packages are fabricated in lab scale. However, the same principle can be applied when there is a need of stacking multiple packages, e.g, 6, 8 or more.

Chapter 6

Conclusion and Outlook

With the basic concept of conventional Ultra-Thin Chip Package (UTCP), Package-on-Package (PoP) and Through-Silicon-Via (TSV), a 3D-stacking technology is developed and discussed in this dissertation work. To avoid the underfilling and package warpage issues in a traditional PoP model, a thin film based packaging and lamination technology is introduced. The packaging technology (UTCP) enables fabrication of flexible electronic packages with metal fan-out. This gives a relaxation on the restriction of making through-hole-vias (THVs) on the high pitch outer contact pads, unlike the TSVs.

The different materials within the stack build-up and their properties (derived from data sheet) are discussed in the chapter 2. During the initial technology development phase, the lamination parameters for uniform adhesive (Pyralux LF 100) flow are optimized and its adhesion strength with respect to other materials in the stack are verified. For making interconnections within the stacked packages, through hole vias are made on the stacked outer-contact pads of the packages. This is done by drilling THs by use of Nd-YAG laser with a trepanning mechanism. A critical factor encountered in this process was the excessive melting of the adhesive layers within the stack due to residual heat. The laser parameters are optimized upto certain extent for getting smooth TH wall.

For the demonstrator fabrication, the packages are out-sourced from one of the TIPS project partners. All these packages are produced with the concept of conventional UTCP (2-layered Polyimide). This leaves a topographical differences of $\sim 15\mu m$ at the edge of thin chip. Although this factor does not affect the package functionality, a drastic reduction in stack yield is observed after laminating 4 layers of such packages. A detailed discussion on the failure analysis of this stack is made in the last part of chapter 3. In this case the average UTCP yield per panel is measured as $\sim 83.5\%$ and the theoretical stacking yield of 52% is verified by the measured value of 46%. However the actual yield of the whole process is found to be only 7%. This implies the stacking process yield (for laminating conventional UTCPs) to be 15%. This failure analysis opens different ways to improve overall yield of the process.

To avoid the die-cracking issue during lamination, the package has to be flat at the chip edge. This is done by introducing an additional polyimide layer with the same thickness as the thin chip thus resulting in "Flat-UTCP". Different generations of Flat-UTCP have been developed and are reported in chapter 4. However none of them are optimized well enough for large scale production which is one of the requirements of stacking principle, to reduce the fabrication cost.

In this dissertation work, the fabrication of Flat-UTCP on carrier of larger dimension (e.g., 4" glass carrier) is considered. This is the minimum size of the released flex, containing many packages that can be laminated using dedicated lamination tool. However, due to the high CTE of polyimide material which is used for Flat-UTCP processing, the whole package shrinks after release. This makes it difficult to fix them within lamination plates by mechanical alignment. Therefore, some investigations are done to control this package deformation after release from carrier. In addition to that, precise placement of thin chip and complete bonding by using BCB as adhesive glue are optimized. A reproducible void-free, well-aligned ($\sim 10\mu m$) thin chip bonding process has been developed.

The 3D-stacking approach including Flat-UTCP technology is demonstrated in chapter 5. As discussed in section 3.5, a single faulty package per stack can make the whole stack non-functional. If the number of faulty packages per panel can be accumulated at one position during the PoP alignment process, the yield of the process improves. By introducing rotational symmetry in the package distribution per panel, selective alignment of functional packages becomes possible. This helps in eliminating the non-functional ones by rotation. As a result, it helps in reducing the number of non-functional stacks. In the current thesis work, the stack includes only 4 chip packages of same dimension and different metal layout. An orthogonal symmetry in package distribution is employed for this particular case. The same concept is useful in stacking higher number of packages in which the multiple chip packages can be fabricated with a rotational symmetry in the packages per panel.

The stacking process yield by using Flat-UTCP has been found to be 83% where as the figure for conventional UTCP case was found to be 15%. Although the yield improvement concept has been proven by introducing Flat-UTCP, still there are some processing issues that can be worked out in future. It includes package deformation which interferes the large area production process of Flat-UTCPs. Also the salt based release process is affected by wet processing. An alternative release process is needed to avoid this difficulty. Laser assisted release of UTCPs by glass-PI debonding may solve both the issues. Some investigation on this release process has been initiated at our CMST group and is being discussed in Section 6.1. More investigation on stress-relief pattern on PDPI HD4110 can reduce the package deformation.

Reliability test of the stacked UTCP containing interconnection test chips can give added value to this technology for future reference. This test includes JESD22-A113E

standard thermal cycling (TC) and moisture sensitivity level (MSL) of the stacks. The focus in these tests is on the THV interconnection which includes copper adhesion onto different types of material. The change in interconnection (Daisy Chain) resistance can give a quantitative measure of degradation during this reliability test. However, the current die bonding process is not optimum and the most risky process which affects the overall UTCP process yield. To perform the reliability test of the stacks, a huge number of thin package stacks are required. As per the current die assembly technology, it is difficult to fabricate the stack within the limited time frame. The reliability test result can be compared with other industrial level packaging technologies after development of proper die-bonding technology. This included precise face-up placement of thin chip and the bonding process.

Thermal management of electronic devices demands the study of thermal behavior of such thin stacks. A test vehicle including fabrication of Thermal (enhanced) UTCPs and their stacks are designed for the measurement of heat dissipation in the thin stack. The fabrication and measurement results are going to be reported in near future. A detailed explanation of the stack design to make the thermal analysis of the thin electronic module is given in Section 6.3.

6.1 Initiative: Laser-assisted package release

The current UTCP process includes a number of wet processing along with salt as release layer. It has been experimentally proven that PDPI HD4110 is more prone to water uptake compared to its counter part, standard polyimide PI2611. Using PDPI HD4110 as the base PI layer sometimes makes it difficult to process it in large substrates. It adds the risk of early package release. This needs a development of new package release technology.

The laser-assisted release process developed by IBM [80] has the capability to release polyimide-metal multilayer. In this process, a sacrificial thin polyimide layer is spin-cured on the optically transparent quartz carrier. After the fabrication process, backside laser radiation with right set of parameters can transmit through the quartz ablating only the sacrificial layer. This concept is being used in many of thin film based research and micro-fabrication processes since past decades [81]–[84].

A trade-off between the optical absorption in the release layer material and the optical transmittance through the carrier material must be carefully considered for the selection of UV laser. Since the laser beam area is normally small, fast scanning is necessary to accelerate the release process for large area samples to be debonded. The laser fluence should exceed the threshold to break the molecular bond at the adhesive to bonded surface interface.

One of the de-bonding concepts includes HD3007 from HD Microsystems as release layer [83]. Its absorption spectrum shows that wavelengths $< 248nm$ are fully absorbed within a $200nm$ thick film of HD3007. Above a certain value of energy

fluence the material is decomposed within this zone and the bond layer is opened. This can be ablated using $248nm$ excimer laser through the glass carrier with high transmittance. In this case, the de-bonding zone is located $200nm$ behind the carrier surface and never closer to the active area which is attached on the other side. Figure 6.1 shows the principle work flow of the excimer laser induced de-bonding approach. The residues both on the wafer and glass are cleaned by a stripping agent for HD3007 which is compatibility both to metals and cured polymers.

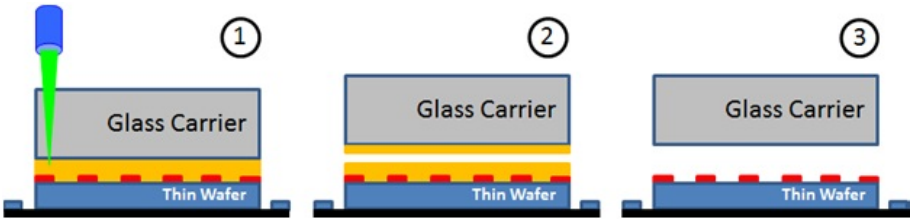


Figure 6.1: Principle work flow of laser induced de-bonding by [83]

The current UTCP process includes white float glass of thickness $0.7mm$ as carrier and PDPI HD4110 as the first layer spin-coated on it. The excimer laser used in our CMST group is KrF-based having a characteristic wavelength (λ) at $248nm$. The transmission curves (T% vs λ) for the float glass is given in the material specification list of PGO. The UV-transmittance range for various thickness of the glass can be found in [85] and [42]. Some of these ranges ($T = 5 - 90\%$) are extracted from Figure 6.2 and are listed in Table 6.1.

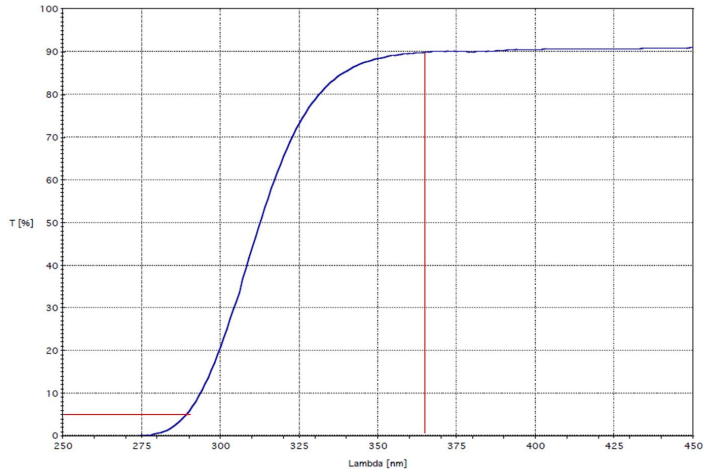
According to Beer–Lambert law (Equation 6.1), the transmittance of a material is dependent on its attenuation coefficient (α) and thickness (which is the path length of the radiation). For a particular wavelength of radiation, the transmittance value decrease exponentially with the thickness of the material.

$$T = \exp^{-\alpha.t} \tag{6.1}$$

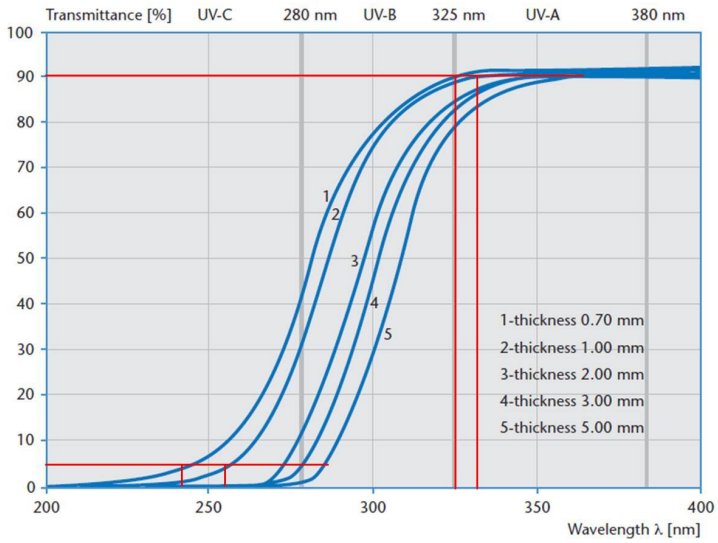
From equation 6.1 and table 6.1 , it is clear that transmittance through $0.7mm$ thick white float glass is almost negligible at the UV-wavelength of $248nm$. The exact value cannot be calculated from the transmittance curve given in the data sheet (as the λ range is from 250 to 450nm for $0.4mm$ thick glass). When a polyimide layer is applied on this type of carrier, the possibility of the transmitted radiation interacting at the polyimide-glass interface is very low. As a result the debonding mechanism with excimer laser will not work by use of this type of glass. And this has been experimentally verified in initial trials. However, the approximate T% for the available Borosilicate glass (thickness $0.5mm$) can be derived from the graph shown in Figure 6.2-b and equation 6.1 which is $\sim 18\%$ for $\lambda = 248nm$.

Borosilicate glass from Schott Jena Glas [42] is manufactured by microfloat process. Its

excellent transmission and its very weak fluorescence intensities over the entire light spectrum make it for a wide range of applications in optics, optoelectronics, photonics and analytical equipment. The transmittance range extracted from the T vs λ curve for this glass of varying thicknesses are given in Table 6.1.



(a) For white float glass of thickness $0.4mm$



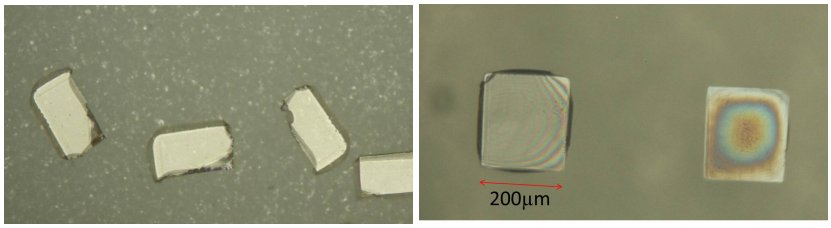
(b) For Borosilicate glass of varying thicknesses (from $0.7mm$ to $5mm$)

Figure 6.2: Transmittance in UV Range (a) For white float glass of thickness $0.4mm$ [85], (b) For Borosilicate glass of varying thicknesses (from $0.7mm$ to $5mm$) [42]

Table 6.1: UV-wavelength (λ) corresponding to Transmittance (T%) range of glass, extracted from [42], [85]

Glass thickness	T% range	$\lambda(nm)$ range
White Float ($0.4mm$)	5-90	290-365
Borosilicate ($0.7mm$)	5-90	245-325
Borosilicate ($1.0mm$)	5-90	255-330

Preliminary experiment was set to debond the $20\mu m$ thick PDPI 4110 spin-cured on the $0.5mm$ thick borosilicate glass (4 " wafer). In this case, the debonding takes place due to local decomposition of the PI film at the glass/PI interface. The decomposition is generally accompanied by the generation of a vapor pressure and is localized by the finite size of the laser beam [84]. This localized pressure can cause a variety of deformations and create localized stresses that can, in turn, introduce defects and cracks. For instance, for PI film under stress due to CTE mismatch with the carrier, the films may buckle away from the substrate without damage. Or, if the pressure is too great the film may bulge and put the film under biaxial tensile stress that can motivate cracking. This needs a very fast scan speed for efficient debonding, eliminating such type of defects and cracks.



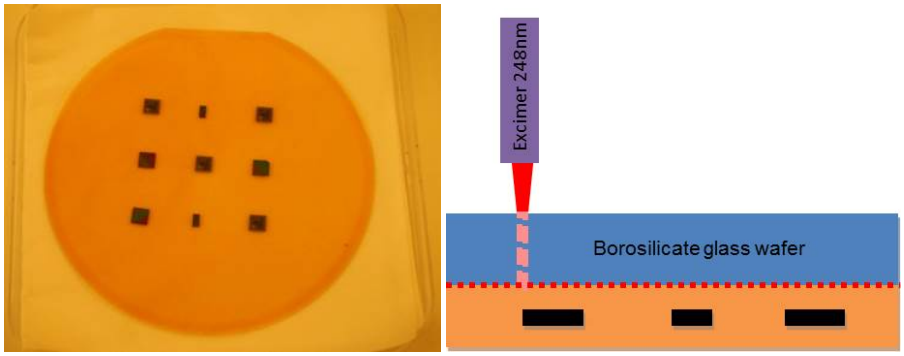
(a) (b)

Figure 6.3: Result of single shot (a) $350mJ/cm^2$ fluence: pieces of PI film collected on a carrier, (b) $300mJ/cm^2$ (left) and $200mJ/cm^2$ (right)

Excimer laser of characteristic wavelength $248nm$ was used with $2000 \times 2000\mu m^2$ mask, demagnification 10 , resulting beam spot of size $200 \times 200\mu m^2$. The 1st trial was to optimize the laser fluence with a single pulse at a place to release the PI from the glass wafer. At the maximum fluence of $350mJ/cm^2$, the PI film is "blown away" from the substrate from the area where the beam is illuminated (Figure 6.3-a). The energy applied here is above the threshold value for the PI film which facilitates the momentum transfer to the film. This is the basic idea behind introduction of the Laser-Induced Forward Transfer (LIFT) technique in which the film is transferred from one carrier on another by forward movement [76]. As shown in Figure 6.3-b, the PI is bulging up or almost detached from the carrier at the fluence $300mJ/cm^2$ where

as unfinished debonding processed can be predicted by looking at the spot made by $200mJ/cm^2$ fluence.

To release the PI of UTCP dimension, 2 pulses of $200mJ/cm^2$ fluence with a fast scanning speed is enough. Lowering the fluence less that $200mJ/cm^2$ needs more pulses at a place. To make the release faster, the pulse frequency and the pulse overlap width have to be high and low, respectively. Increasing the frequency from $100Hz$ to $300Hz$ reduces the total ablation time with negligible change in surface morphology of the released layer. However lowering the pulse overlap width reduces the easy release probability.



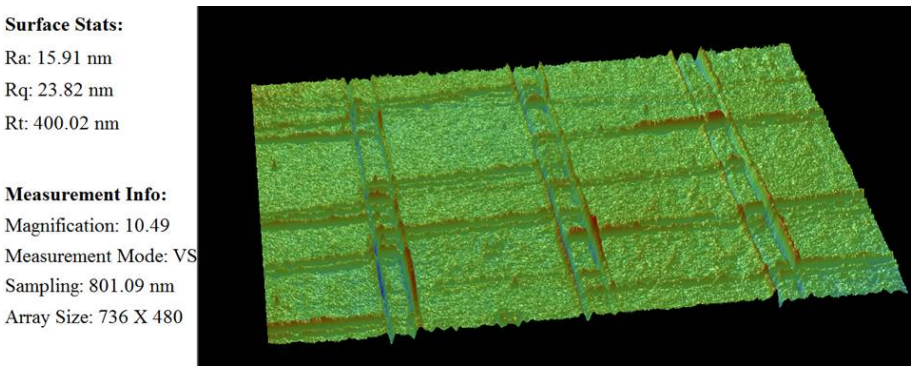
(a) (b)

Figure 6.4: (a) PI-Chip-PI (Flat-UTCP assembly) processed on 4 " borosilicate glass wafer, (b) Schematic cross-section showing glass-PI interface (red dotted line) where the debonding takes place by laser radiation

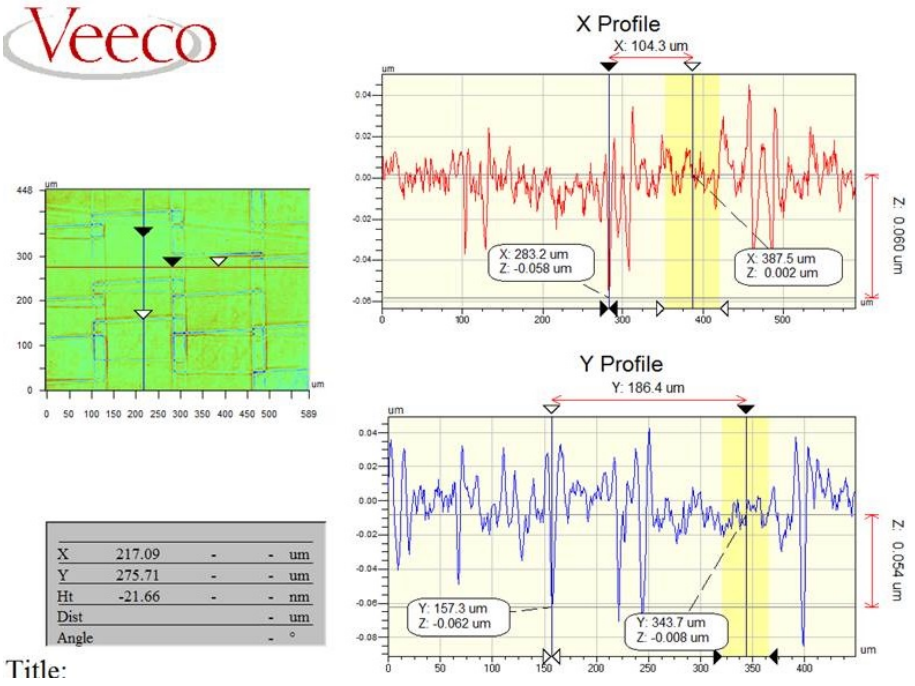
To demonstrate the UTCP release process, an assembly of multi-chip flat packages is processed on the 4 " borosilicated glass wafer using the developed process flow based on PDPI HD4110. Figure 6.4-a shows the top view of the sample used for the laser release experiment. It includes dummy silicon chips of thickness $30\mu m$ and different size: $5 \times 5mm^2$, $2 \times 4mm^2$. The schematic of interface area in this process is shown by red dotted line in Figure 6.4-b.

To release single UTCPs (each containing one chip) from the carrier, a contour of requisite UTCP size is defined on the PI (off-chip). This is done by ablating it with high power before starting the actual debonding process. Generally the UTCP area includes chip size plus additional area at the periphery upto $5mm$ for metal fan-out realization. For the dummy chip of size $5 \times 5mm^2$ and $2 \times 4mm^2$, the area per each UTCP are fixed as $15 \times 15mm^2$ and $12 \times 14mm^2$, respectively. The Excimer laser parameters used for this cutting process are 2 pulse at a place with fluence $\sim 900mJ/cm^2$ and scanning speed $10mm/s$. The debris at the cutting edges are cleaned by N_2 blow. The sample is again mounted on the laser stage with face down and realigned on the ablated

contour.

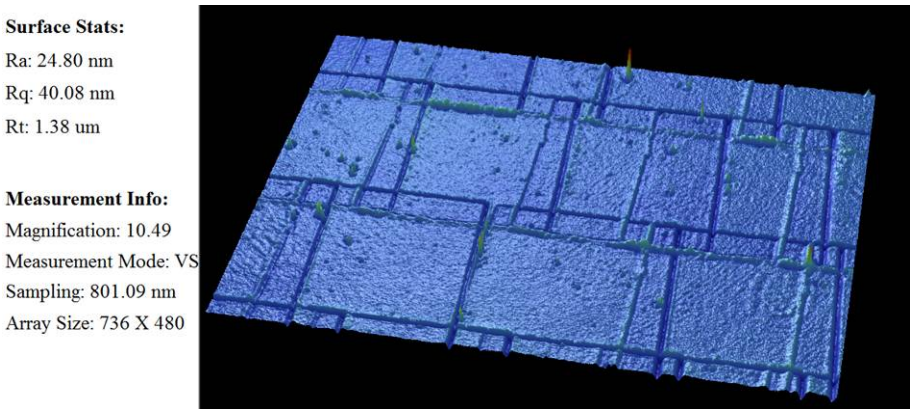


(a)

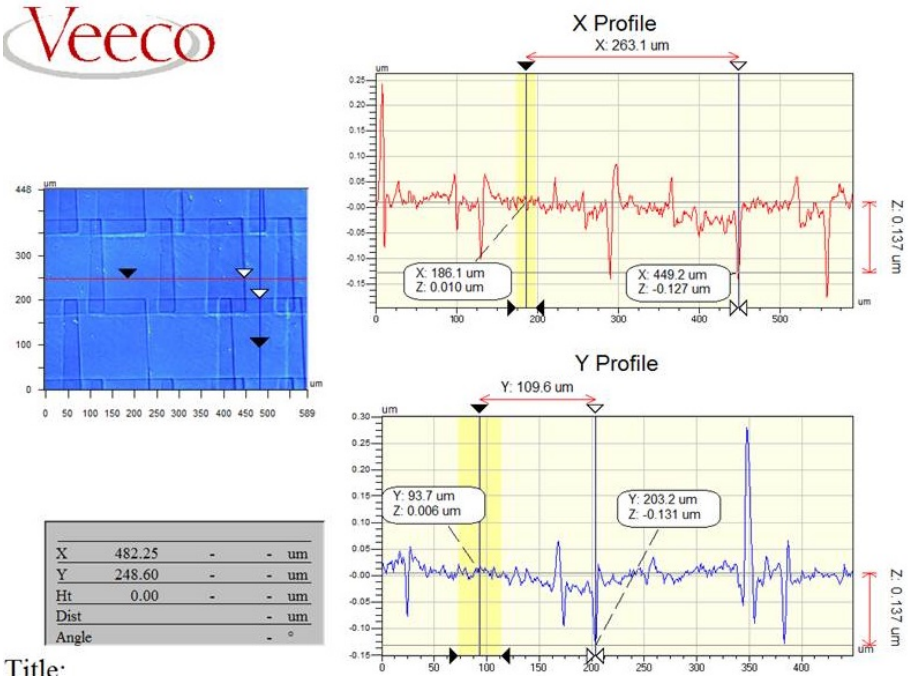


(b)

Figure 6.5: Wyko analysis showing surface morphology of the polyimide side after release by laser debonding process (2 pulses, fluence $200mJ/cm^2$, $20\mu m$ pulse overlap width), (a) 3D view, (b) 2D view showing roughness



(a)



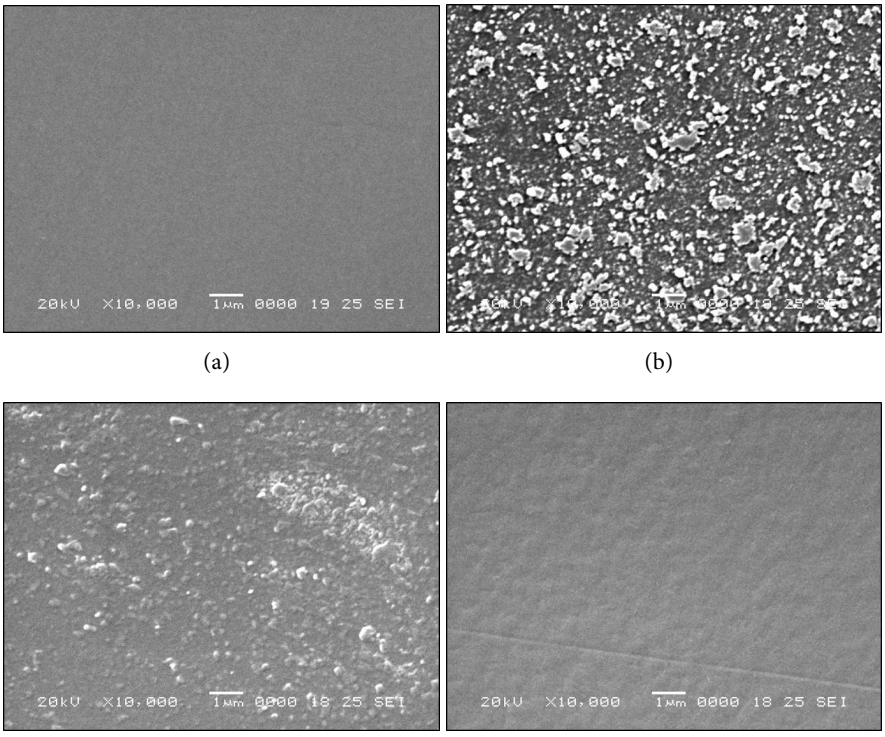
(b)

Figure 6.6: Wyko analysis showing surface morphology of the polyimide side after release by laser debonding process (2 pulses, fluence $230mJ/cm^2$, $20\mu m$ pulse overlap width), (a) 3D view, (b) 2D view showing roughness

The packages with two different dimensions (in this particular case) are scanned at a speed of $10mm/s$, frequency $300Hz$ with 2 pulses per location. The laser fluence used for scanning the area of $15 \times 15mm^2$ and $12 \times 14mm^2$ dimension are $\sim 200mJ/cm^2$

and $\sim$ $230mJ/cm^2$, respectively. A slight increase in fluence ($\sim$ $200mJ/cm^2$ to $\sim 230mJ/cm^2$) is made to make the release process easier for the 2nd case.

All the packages are released successfully with minor changes in the surface of the PI facing the surface. This can be verified through the wyko analysis (Figure 6.5 and 6.6) of the PI side after release from the carrier. A change in the released sample area which in turn changes the laser fluence from 200 to 230 mJ/cm^2 leads to increase in PI surface roughness (R_q) from $24nm$ to $40nm$. In both the cases, the pulse overlap width was fixed at $20\mu m$. Due to additional pulse at this region, trenches of depth 60 and $130nm$ can be noticeable, respectively.



(a) (b)

(c) (d)

Figure 6.7: SEM image with X 10k magnification of the interface side of glass and PI after release (a) Clean glass carrier (for reference), (b) Laser ablated glass carrier, (c) Polyimide surface (off-chip), (d) Polyimide surface (on-chip)

The cleanliness of the released side is verified by SEM-EDX analysis. For making reference to material content and/ or surface smoothness, a clean borosilicate glass is first analyzed. After debonding process, the glass surface becomes highly rough which can be seen in Figure 6.7-b. EDX analysis to count the mass percentage of the

surface elements does not confirm the presence of PI residues on the carrier. Same is the case for PI side where residues of glass can be expected. One interesting thing is observed in this analysis, that is PI surface roughness is different at two different regions: on-chip and off-chip (Figure 6.7-c,d). The PI surface below the chip has higher smoothness as compared to the off-chip region. The only difference is that the chip is bonded on the base PI by applying a pressure of 2 bar/die which is not not the case in rest part of PI. Although this base PI layer is processed by a single spin-cured step, the surface in both the parts gets different morphology after the debonding process.

The release process can be made more faster by using ps or fs laser which is currently operational in our group. More investigation can be done in developing this process by releasing UTCPs of larger dimension. As both the carrier material and release process are different, the difficulties in the current UTCP processing (wet processing issues) can be reduced upto certain level.

6.2 Future Work 1: Chip-on-Carrier

Multiple chip placement is the most risky and time consuming step in the whole production process. It can be made more easy by introduction of new process, *"Chip-on-Carrier"*. In this case, the thin chip as used for face-up placement can be attached to a temporary carrier via a temporary adhesive. The whole combination will act as a pseudo-thick chip which can be picked and placed precisely by a fine placer using flip-chip principle. After complete bonding of the chip on the PI substrate, the temporary carrier together with the adhesive material can be easily removed. All these steps has to be developed to avoid the risk of getting void under the non-flat thin chip during placement and BCB overflow on the thin chip in the curing process which has been discussed in great details in chapter 4-5.

6.3 Future Work 2: Thermo-mechanical Analysis of Stacked UTCPs

In the initial phase of TIPS project, the thermo-mechanical behavior of the UTCP was verified by use of PDPI HD4110 based 2-layered conventional packages. The mechanical measurement includes tensile strength analysis of $20\mu m$ thick polyimide film and bowing of the whole assembly after each process step. As the process was not developed up to the standard, the result cannot be used for future reference.

The thermal measurement needs a thermal test die to be packaged as a UTCP and study the thermal behavior of the whole package by using different dummy heating planes. After the measurement, four of these packages can be stacked vertically producing stacked UTCPs. The through hole interconnection on the fan-out metal contact of the stacked thermal UTCPs enables the thermal measurement of each package within

the stack. A dedicated thermal test chip (PTCL), designed and manufactured by IMEC, is used for making this measurement.

6.3.1 PTCL test dies

PTCL is the abbreviated form of Packaging Test Chip version L. The capability to generate heat and to measure temperature makes PTCL suitable for thermal characterization of dies and materials; by placing them into a sandwich made of 2 PTCL matrices, on top and bottom respectively, and using (for example) the bottom as heater and the top as thermometer, one can evaluate the heat propagation and the thermal resistance of the material/die under test.

The unit die, Figure 6.8, is composed of one heater and 2 thermometers. The heater is divided in 4 quadrants; each heater quarter is connected in series with the other 3. The 2 thermometers are placed in the top-left corner and in the center of the die. The heater in each unit die is designed to have a resistance of $\sim\ 111\Omega$, in order to deliver $10W$ with the maximum current of $300mA$, which can be injected through 3 contact pads in parallel ($\sim\ 100mA$ max for each) attached to the large heater pads. The 2 thermometers of PTCL are 4-terminal n+p diodes. The layout is in Figure 6.8-b. The use of these diodes as thermometers requires forcing a constant current through the current terminals and measuring the voltage drop at the voltage terminals, Figure 6.8-c. The dependency of the voltage drop on temperature is given by dV/dT = $-2mV/°C$. The whole concept of measurement is adopted in making circuit design for the UTCP packages, followed by stacked package design.

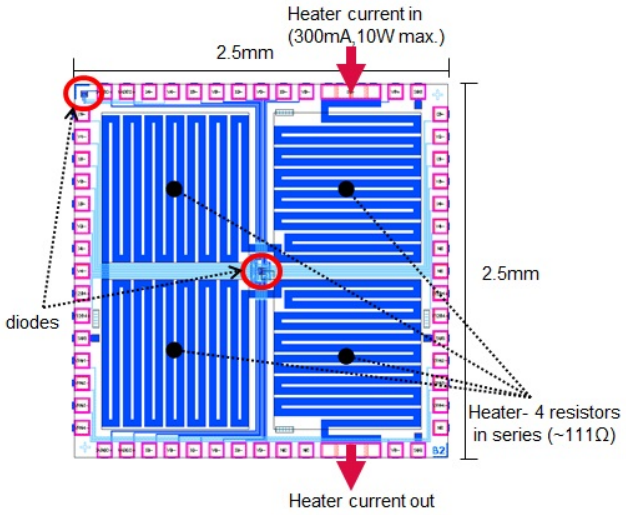
The PTCL chips from IMEC are available in the form of un-thinned diced wafer. As per the current process flow, the precise placement of chip in multi-UTCP fabrication is realized via flip-chip placement principle with an accuracy of $\sim\ 10\mu m$. In this case, the backside edge of the thinned silicone chip is allowed to match the alignment pattern on the substrate. Before making the whole design, the exact size of the chip including the excess area as chip border is being measured to rescale the alignment mark for chip placement.

Figure 6.9-b shows the PTCL chip layout in the Clewin design file. The actual size of the chip is $2.5 \times 2.5mm^2$ with having 60 contact pads. The pad and pitch size are $100 \times 100\mu m^2$ and $150\mu m$, respectively. The diced PTCL chips have an additional width of $\sim 80\mu m$ which has to be taken into account in making the complete design file.

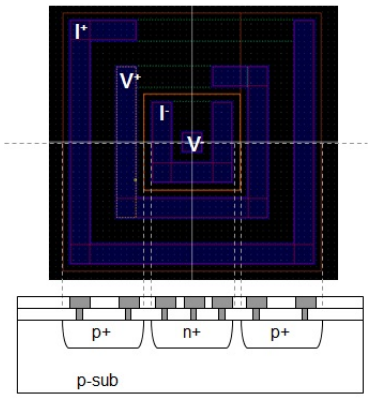
6.3.2 Package design

The metal fan-out for the UTCP is designed in such a way that the thermal measurement of individual package can be made even after stacking four of these packages. For the specific application, this package is termed as *"Thermal UTCP"*. Each of the PTCL package in the stack contains 8 fan-outs: four points (I-V input-output)

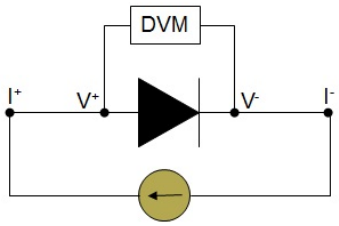
each for heater and thermometer. The fan-out contact pad are arranged in a symmetric way to minimize the package size and reduce the cost of mask making.



(a) Layout of PTCL chip

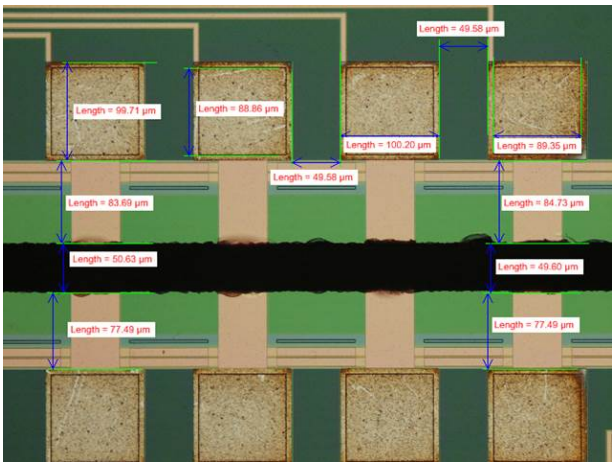


(b) The internal layout of PTCL chip

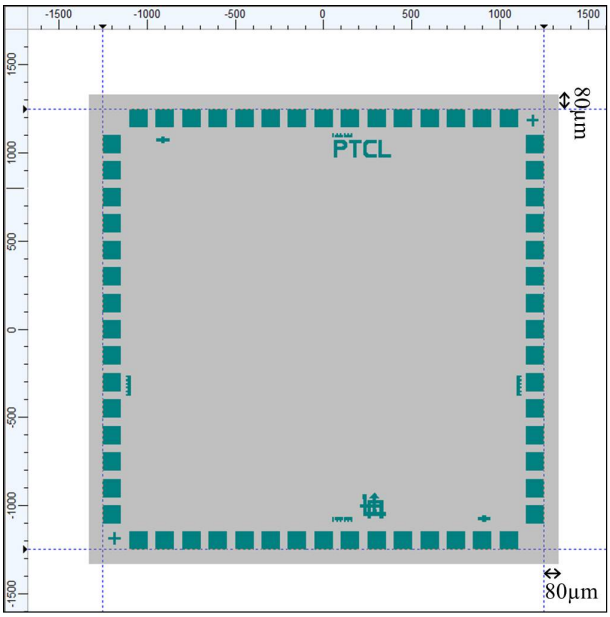


(c) Electrical configuration for temperature measurements

Figure 6.8: (a) Layout of PTCL chip, (b) The internal layout of PTCL chip, (c) Electrical configuration for temperature measurements



(a) Diced edge of PTCL chip showing the contact pad size and additional $\sim 80\mu m$ width at the chip edge

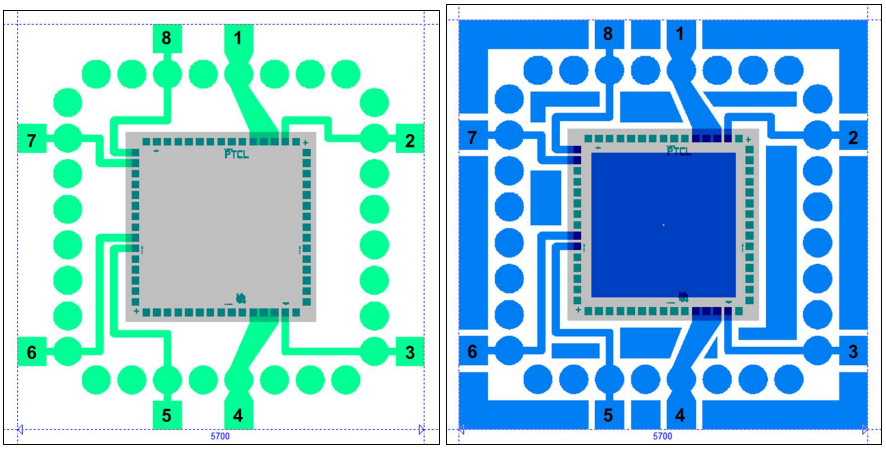


(b) PTCL chip layout on design file including the chip edge which is a factor of concern during chip placement

Figure 6.9: (a) Diced edge of PTCL chip showing the contact pad size and additional $\sim 80\mu m$ width at the chip edge, (b) PTCL chip layout on design file including the chip edge which is a factor of concern during chip placement

The metal layout for the PTCL package is shown in Figure 6.10. This design contains

32 circular pads (8 on each side) of $400\mu m$ diameter and $500\mu m$ pitch for making TH- interconnection after stacking these packages. The 8 measurement points (Figure 6.10-c) are distributed at the 4 sides of the package (2 on each side). Their positions are allocated to avoid the overlapping these points by a sequential 90°rotation of the packages with same layout. As a result the 4 UTCPs with same metal layout can be stacked together by making 90°rotation in the succeeding layers before stacking them by lamination.



(a) Layout of thermal UTCP based on PTCL chip

(b) Layout of thermally enhanced UTCP with additional metal outlines

1. IR+ , 2. VR+, 3. VR-, 4. IR-, 5. V1+, 6. I1+, 7. V1-, 8. I1-

(c) Probe points on the design (a, b) for thermal measurement

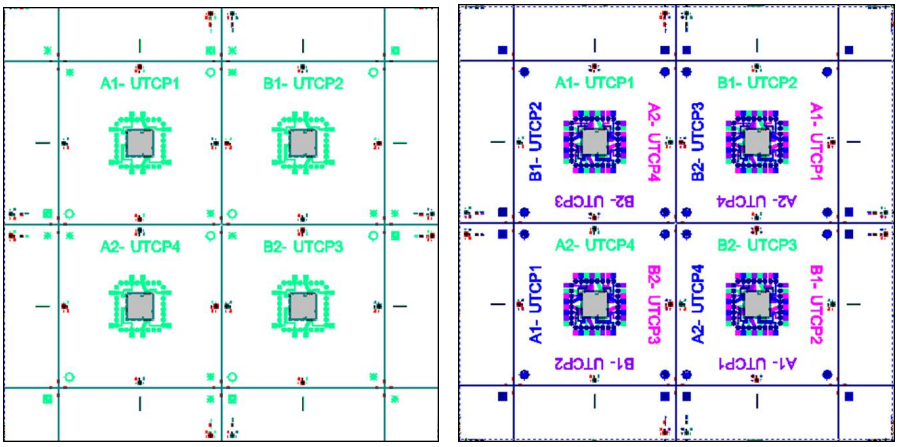
Figure 6.10: (a) Layout of thermal UTCP based on PTCL chip, (b) Layout of thermally enhanced UTCP based with additional metal outlines, (c)The probe points for thermal measurements

For applying maximum current to the heater, the 3 contact pads at each end of the heater are connected together making a single copper track of higher width (point 1 and 4). The 4th contact pad (point 2 and 3) can be used for measuring the voltage drop across the meander shaped heater. Point 6 and 8 can be used for applying constant current to the diodes. Point 5 and 7 allow to measure the voltage across the diodes from which the thermal characteristic of the whole package can be derived.

PDPI HD4110 facilitates the Flat-UTCP process with photo-via formation on contact pads of the chips. The micro-vias of size $60 \times 60\mu m^2$ have the tolerance of $\pm 20\mu m$ misalignment in the current design of process flow. All the copper tracks in the circuit are of width $100\mu m$. The measurement pads are squares of size $400 \times 400\mu m^2$ and are located at the outer side of the TH pads to avoid the risk of damaging the copper

track before stacking.

Among all the materials present in the current version of the UTCP, copper has highest thermal conductivity than other layers. To see the effect of heat spreading layer in the thermal measurement, another layout is designed which includes more copper area per package. The package containing higher copper volume is named as *"Thermally Enhanced UTCP"* and the metal layout is illustrated in Figure 6.10. As per the design, the copper area per package of size $5.7 \times 5.7mm^2$ is calculated as $3.1 \times 10^6 \mu m^2$ and $21 \times 10^6 \mu m^2$ for Thermal UTCP and Thermally Enhanced UTCP, respectively.



(a) Layout of four Thermal UTCPs in 2 x 2 matrix form

(b) Top side view after stacking 4 of these UTCP layouts with making a sequential rotation of 90° in each layer

Figure 6.11: (a) Layout of four Thermal UTCPs in 2 x 2 matrix form, (b) Top side view after stacking 4 of these UTCP layouts with making a sequential rotation of 90° in each layer

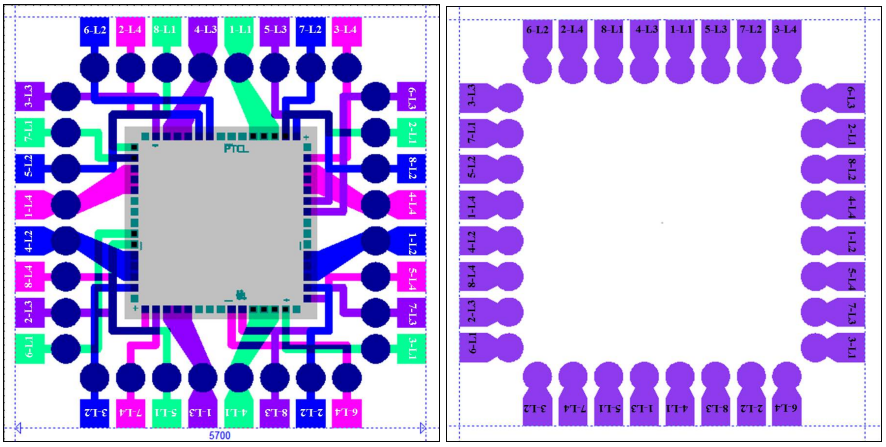
Four of such packages can be processed on a single carrier with acceptable accuracy in position of the thinned chip. Figure 6.11-a shows layout of the 4 Thermal UTCPs arranged in 2x2 matrix form with a symmetry in package positions. After making thermal measurement, they can be released from the carrier as a single layer containing 4 packages. 4 of such layers can be aligned on top of each other with a sequential rotation of 90° (Figure 6.11-b).

The Thermally Enhanced UTCPs can also be fabricated with the same principle. The only difference will be copper area per package which has been shown in Figure 6.10. The CTE of copper is high as compared to other materials in the package. Increasing the Cu area per panel of packages can increase the risk of package deformation after release from the carrier. After complete fabrication process, the stack will be diced to

the size of $5mm^2$. This means having dummy planes of copper across the whole panel will not be considered in the final measurement.

6.3.3 Stack design

After stacking the 4 layers, the top-side of a single stacked Thermal UTCPs with all the measurement points can be viewed as Figure 6.12-a. These points allow to make the thermal measurements of the embedded packages. The vertical interconnection within the stacked packages are made by Through hole drilling and plating process. Top and bottom side conductive surface can be patterned using the design Figure 6.12-b which protects the plated TH-vias and patterns the measurement pads. The probe points for thermal measurements are denoted as x-Ly where "x" is the probe points per each UTCP package varying from 1 to 8 (ref. Figure 6.10) and "Ly" stands for four layers (L1 to L4) of UTCP packages in the stack.



(a) Close view of one of the stacked patterns in Figure 6.11

(b) Layout for top and bottom side metal patterning of the stack

Figure 6.12: (a) Close view of one of the stacked patterns in Figure 6.11, (b) Layout for top and bottom side metal patterning of the stack.

Publications

Papers in journals

1. **Swarnakamal Priyabadini**, Tom Sterken, Luc Van Hoorebeke and Jan Vanfleteren, ``3D stacking of ultra-thin chip packages: an innovative packaging and interconnection technology" *IEEE Transactions on Components Packaging and Manufacturing Technology*, vol. 3, no. 7, p. 1114-1122, 2013.

2. **Swarnakamal Priyabadini**, Tom Sterken, Maarten Cauwe, Luc Van Hoorebeke and Jan Vanfleteren, "High yield fabrication process for 3D-stacked ultra-thin chip packages using photo-definable polyimide and symmetry in packages ", *IEEE Transactions on Components Packaging and Manufacturing Technology*, (in press 2013, DOI: 10.1109/TCPMT.2013.2284068)

Papers in conference proceedings

1. **Swarnakamal Priyabadini**, Tom Sterken, Maaike Op de Beeck and Jan Vanfleteren, ``Photo-definable polyimide-based Flat-UTCP technology for 3D-stacking application," *Proc. of Smart Systems Integration (SSI 2013)*, Amsterdam, The Nederlands, March 13-14, 2013.

2. **Swarnakamal Priyabadini**, Tom Sterken, Liang Wang, Kristof Dhaenens, Bjorn Vandecasteele, Steven Van Put, Andreas Erik Petersen and Jan Vanfleteren, ``An approach to produce a stack of photo definable polyimide based flat UTCPs," *Proc. of 4th Electronics System Integration Technologies conference (ESTC 2012), IEEE*, Amsterdam, The Netherlands, October 17-20, 2012.

3. Tom Sterken, Maaike Op de Beeck, Filip Vermeiren, Tom Torfs, Liang Wang, **Swarnakamal Priyabadini**, Kristof Dhaenens, Dieter Cuypers and Jan Vanfleteren, ``High-yield embedding of $30\mu m$ thin chips in a flexible PCB using a photopatternable polyimide based ultra-thin chip package (UTCP)," *Proc. of 45th International Microelectronics Assembly and Packaging Society (IMAPS 2012)*, p. 940-945, San Diego, CA, USA, October 9-13, 2012.

4. **Swarnakamal Priyabadini**, An Gielen, Kristof Dhaenens, Wim Christiaens, Steven Van Put, Gerhard Kunkel, Anders Erik Petersen and Jan Vanfleteren, ``3D-stacking of UTCPs as a module miniaturization technology," *Proc. of*

44th International Symposium on Microelectronics, Proceedings. International Microelectronics and Packaging Society (IMAPS 2012), p. 463-468, Long Beach, CA, USA, October 9-13, 2011.

5. Thomas Loeher, David Schuetze, Wim Christiaens, Kristof Dhaenens, **Swarnakamal Priyabadini**, Andreas Ostmann and Jan Vanfleteren. ``Module miniaturization by ultra thin package stacking," *Proc. of 3rd Electronic System Integration Technology conference (ESTC 2010), IEEE*, Berlin, Germany, September 13-16, 2010.

Other Achievement

1. "Outstanding Student Paper Award" for the paper “3D-Stacking of UTCPs as a Module Miniaturisation Technology”, at 44th International Symposium on Microelectronics (IMAPS 2011), Long Beach, CA (USA), October 9-13, 2011.

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